A Tracking ADC with Transient-Driven Self-Clocking for Digital DC-DC Converters

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Zusammenfassung

Mit zunehmender Skalierung der CMOS Technologie werden Rauschen, Mismatch und Prozessabweichung zu einer Hauptbeschränkung in DC-DC Konvertern. Deshalb wird der digital unterstützte DC-DC Konverter als Alternative in neu entwickelten System bevorzugt. Digitale DC-DC-Konverter sind nicht nur viel einfacher zu konfigurieren, sondern noch robuster gegen Rauschen, Störung und Prozessschwankungen.

Als ein Interface-Bauelement zwischen analoger Welt und digitalem Signal Prozess, müssen die ADCs für den Einsatz in digitalen DC-DC Konvertern optimiert werden. Die üblichen synchronen ADCs, wie SAR und Pipeline ADCs, brauchen mehrere Taktperioden für eine Konvertierung, und sind daher nicht geeignet für die Anwendung in DC-DC Konvertern. Um den Konverter stabil zu halten, erfordert die digitale Rückkopplung in DC-DC Konvertern eine sehr kurze Gruppenlaufzeit (Totzeit). Deswegen müssten synchrone ADCs sehr hoch getaktet werden. Dies würde dann aber auch eine hohe Verlustleistung nach sich ziehen.

Im Vergleich hierzu hat der Zähler-Rampe oder Tracking ADC die kürzeste Gruppenverzögerung, indem die Konvertierung innerhalb einer Taktperiode durchgeführt wird. Damit kann das Ausgangssignal zeitlich von der digitalen Rückkopplung entnommen werden und die Regelung schnell reagieren. Trotzdem müssen synchrone Tracking-ADCs doppelt so schnell getaktet werden wie die Bandbreite des Rauschens und der Störungen. Deswegen hat auch dieser ADC mehr Leistungsverbrauch als unbedingt erforderlich.

In dieser Arbeit wird ein neues Konzept für Tracking ADCs präsentiert, deren Konversionsgeschwindigkeit automatisch von der Flankensteilheit der Eingangssignale bestimmt wird. Das heißt, wenn sich das

Eingangssignal langsam ändert, wird dieser ADC auch langsamer getaktet. Aber wenn das Eingangssignal sich schnell ändert, z. B. bei Transienten, wird der ADC sofort schneller getaktet werden, um dem Eingangssignal präzise zu folgen. Mit diesem Konzept werden nicht nur die Überlast beim Verfolgen von Transienten herabgesetzt, sondern auch noch die durchschnittliche Abtastrate reduziert. Folglich wird die Verlustleistung des ADCs deutlich reduziert.

Zum Nachweis dieses Konzeptes wird ein 6-bit Tracking ADC mit transienten-gesteuertem Takt in einer 130 nm CMOS Technologie implementiert. Der Prototyp des ADCs besitzt die Fläche mit $400 \times 200\,\mu\text{m}^2$. Die maximale Verlustleistung ist $84\,\mu$W bei 1,4 V Versorgungsspannung und einer Abtastfrequenz von 50 MS/s. Die integrale Nichtlinearität ist besser als 0,5 LSB, und die effektive Auflösung (ENOB) bei der Abtastfrequenz vom 12,5 MHz ist 4,4 Bit, wobei die ideale ENOB 5 Bit wäre.

Abstract

With further scaling of CMOS technology noise disturbance, mismatch and process variation become the major constraints of analog DC-DC converters. Consequently, digitally assisted DC-DC converters are coming in the focus of new systems, because they are easier to be configurated in the applications than the typical analog DC-DC converters, while being more robust against noise disturbance and process variation.

As interface devices between analog real world and digital signal processing, ADCs must be optimized for signals in digital DC-DC converters. But the existing synchronous ADCs, which require multiple clock cycles per conversion, as SAR and Pipeline ADCs, are not suitable for the application in DC-DC converters because of special signal characteristics. For stability reasons the digital feedback control in DC-DC converters requires a short group delay (dead time). So synchronous ADCs must be run at a sampling frequency as high as possible. But this approach results unfortunately in high power dissipation.

Compared to the above mentioned ADCs, the delta-encoded or Tracking ADC exhibits the shortest group delay by performing the data conversion only in one clock cycle. It makes the digital feedback control of DC-DC converters possible to response the output exactly and simultaneously. However, the synchronized Tracking ADC still has to cover the double of broad signal bandwidth of disturbance, which appears at the output of DC-DC converters occasionally, dissipating unnecessary excessive power.

This dissertation presents a new concept of Tracking ADC that self-adjusts the conversion rate depending on the slope of the input signal. For a slowly varying input, this Tracking ADC is self-clocked at a low

frequency in normal mode, but once the signal varies fast and the slope exceeds a defined threshold, the conversion rate of the ADC is increased to track the signal accurately. By using the proposed solution not only the issue of input slope overload for typical Tracking ADCs is significantly improved, but also the average sampling rate is decreased. Therefore, the power dissipation of the proposed ADC is also reduced.

As a proof of this concept, a 6-bit Tracking ADC with transient-driven self-clocking is implemented in 0.13 μm CMOS technology. The prototype of the ADC occupies an area of $400 \times 200\,\mu\text{m}^2$. The maximum power dissipation is 84 μW at a supply voltage of 1.4 V, when operated at 50 MS/s. The integral nonlinearity (INL) is better than 0.5 LSB, and the effective number of bits (ENOB) at the sampling frequency of 12.5 MHz is 4.4 bits, where the ideal ENOB is limited to 5 bits for 6-bit Tracking ADCs.

In memory of my mother

To my father, my wife and children

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Finally, I want to express my sincerest appreciation to my family. They always encouraged and supported me throughout my life, believing in me and in my success. Their unconditional love warmed my heart. This work is dedicated to them!

Contents

List of Equation Symbols

μ_n	Charge mobility	[cm^2/Vs]
C_{out_IDAC}	Output capacitance of current mode DAC	[pF]
G_c	Average gain for linearized comparator	
V_{dd}	Power supply voltage	[V]
$(WL)_{min}$	Minimum area of MOS transistor	[m^2]
$\overline{I_n^2}$	PSD of the noise current	[A^2/Hz]
σ_{DNL}	Standard deviation of DNL	
σ_{INL}	Standard deviation of INL	
A_β	Proportionality constant in terms of process deviation	[$\%\mu m$]
A_{VTH}	Proportionality constant in terms of threshold voltage deviation	[$mV\mu m$]
C_{gd}	Parasitic capacitance between gate and drain of MOS transistor	[pF]
C_{gs}	Parasitic capacitance between gate and source of MOS transistor	[pF]
C_{out}	Output capacitaor	[pF]
$C_{ox}^{'}$	Oxide capacitance per area of MOS transistor	[F/cm^2]
C_{unit}	Output capacitance of unit current source in IDAC	[pF]
f_T	Transition frequency of MOS transistor	[GHz]
$f_{in,max}$	Maximum bandlimited frequency of input signals	[Hz]
$f_{lp(s)}$	Transfer function of low pass filter	
G_m	Transconductance of an inverter in latch	[$\mu A/V$]
g_m	Transconductance of MOS transistor	[$\mu A/V$]
G_{int}	Integrator in dynamic modeling	
g_{m_in}	transconductance of common-source input pair in latched comparators	[$\mu A/V$]
$H_{integrator}$	Frequency response function of integrator	
I_D	Drain current of MOS transistor	[A]
$I_{kickback}$	Kickback noise current	[A]

List of Equation Symbols

I_{unit}	Unit current source in IDAC	[A]
K_P	coefficient of process technology	[$\mu A/V^2$]
k_B	Boltzmann constant equal to 1.38×10^{-23}	[J/K]
r_{lin}	Output resistance of MOS transistor in linear region	[Ω]
r_o	Output resitance of MOS transistor in small signal model	[Ω]
SR	Slew rate	[$V/\mu s$]
T	Absolute temperature	[K]
V_{amp}	Maximum amplitude of input signals	[V]
V_{cmp+}	Positive input of the main comparator in modeling	[V]
V_{cmp-}	Negative input of the main comparator in modeling	[V]
$V_{DS,sat}$	Drain-source saturation voltage of MOS transistor	[V]
V_D	Input differential voltage of latched comparators	[V]
V_{FS}	Full scale voltage	[V]
$V_{kickback}$	Kickback noise voltage	[V]
V_{TH}	Threshold voltage of MOS transistor	[V]
V_{total_n}	Total rms noise voltage	[V]

Chapter 1

Introduction

1.1 Motivation

With the rapid development over past decades hand-held electronics for consumers and communication have become more popular. The influence caused by this development imposes higher demand of power efficiency to electronic devices, which are driven mainly by the battery. Consequently, to increase the power efficiency of portable devices, the supply voltage as well as feature size of MOS transistors need to be scaled further to fulfill the requirement of users and applications as well.

This evolution has controversial issues for digital and analog circuit applications. Enabled by the scaling of integrated technology, the computing devices as DSP or microcontroller made huge progress in this area. With reduced voltage supply and smaller transistor dimensions more transistors can be produced in unit dimension, costing less. Digital circuits with more transistors can perform also more complex algorithms at higher operation speed, but need less power due to reduced voltage supply.

However, advantages to digital circuits do not mean also positive benefit to analog technology. This is due to different requirements for circuit design. For analog circuit, high speed, low distortion and low noise are the priorities, while low power cannot be sacrificed. But the application of all of the requirements to the analog circuit design simultaneously can only results in the trade-off. Fundamentally, high speed means actually high power. The improperly scaled threshold voltage V_{TH} and decreasing supply voltage make the operational range of devices smaller. Although the pure analog circuits benefit also from the technology scal-

ing, particularly in terms of high speed, the limitations of noise, distortion and dynamic range constrain especially the performance over time.

Based on this development, the tendency of using less analog circuits but more digital processing becomes necessary. As interface devices, Analog-Digital converters (ADC) that bridge the gap between analog and digital domains are indispensable for sampling the signal of radio, image and sensor, for instance. But among the broad range of ADCs each of them has its own features. None of them can fulfill all requirements of different applications at the same time. Therefore, the ADC presented here will be specifically designed, considered and discussed for the application of power management.

1.2 Contribution

Driven by the increase in transistor count per generation, power management is now the primary issue across almost all of application segments. In particular, for portable consumer devices and implant devices in the field of human health the limited energy supplied by battery has to be used more efficiently to achieve longer duration.

In the past few years many innovations have been done in the fields of DC-DC converters. Fundamentally, by using current control mode DC-DC converters achieve the efficiency of conversion better than 90 percent. But due to the growing demand of low power and further scaling of CMOS technology, DC-DC converters with analog control feedback go near to the bottleneck of the performance. In addition to the mismatching and process variation of technology, the diminished signal-to-noise ratio (SNR) becomes the major constrains for analog applications. Therefore, digitally assisted DC-DC converters attract more attentions from designer.

However, the digitally assisted DC-DC converters have also their own constraints and limitations, which are group delay or dead time in the control feedback. Principally, the digital control feedback in DC-DC converters comprises one ADC, digital filter and digital pulse-width-modulator (DPWM). In Fig. 1.1 the ADC block replaces the analog error amplifier and produces the digital data, which is processed by successive digital blocks. But the ADC and digital filter blocks cause the group delay or "dead time" in the control theory. If the group

delay is long, the feedback control systems cannot response the disturbance simultaneously. Thus, the group delay caused by ADC and pass filter should be as short as possible. Additionally, to achieve high conversion efficiency in DC-DC converters, the control feedback itself should dissipate less power. Digital circuits consume no static power, but the dynamic power dissipated by digital circuit with increased transistor count per generation and more sophisticated algorithms has to be considered. Based on the above analysis, we can observe that short group delay ("dead time") and less power dissipation are essential and crucial to the applications of digital controlled DC-DC converters.

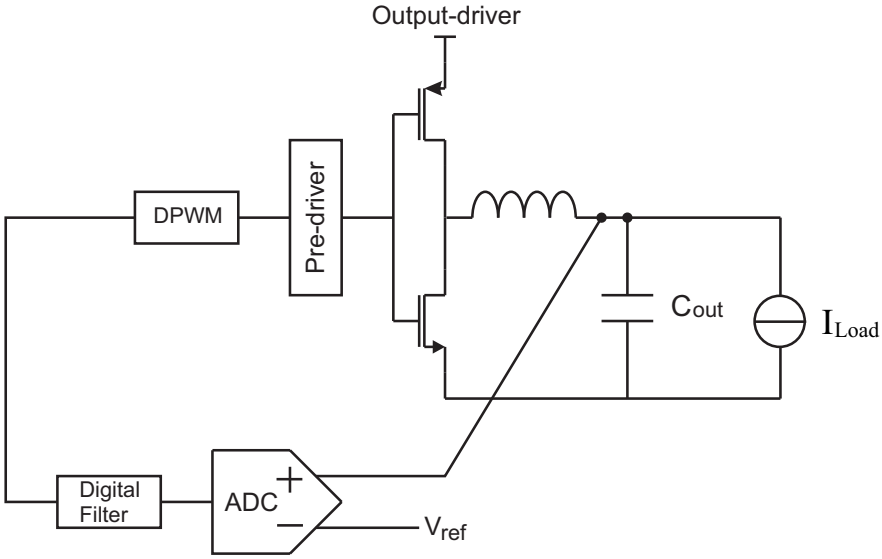

Figure 1.1: DC-DC converter with digital control feedback

Unfortunately the short group delay or high conversion rate with low power is one intrinsic trade-off. More precisely, it is not possible to achieve all requirements simultaneously. If high speed is required, high power has to be provided or supplied.

Many research works for digital controlled DC-DC converters have been published in [1, 2, 3, 4]. In these publications all of them use either Sigma-Delta ADC or Successive Approximation ADC (SAR) to perform the conversion operation. Although Pipeline [5, 6] and Folding-Interpolating ADCs [7, 8] operate very fast, they consume too much power that DC-DC converters can afford. Sigma-Delta and SAR ADCs work upon totally different principles. Sigma-Delta ADCs using decimation average the output of modulator that requires high bandwidth, while SAR approaches the final value binary. But both kinds of ADCs have one

common drawback that the clock frequency must be multiple to their sampling frequency. More precisely, for 6-bit SAR ADC the clock frequency is 6 times its sampling frequency, whereas the clock frequency in oversampling ADC is at least 3 times its sampling frequency just for first-order, according to [9]. These architectures due to their inherent characteristics result in high power dissipation of ADC and long group delay, which are not desired absolutely for the application of power management.

In this thesis a new concept of the ADC is introduced to fulfill the requirements of DC-DC converters, improving the performance of digital control feedback. The data conversion of oversampling ADC and SAR ADC requires multiple clock cycles, which are called "dead time" in the control loop. The longer dead time is, the more instable the whole system becomes. To overcome this issue, delta-encoded or Tracking ADC could be an optimal solution. The architecture of delta-encoded ADC is very simple and partially similar to SAR ADC. Fig. 1.2 shows that the counter feeds the DAC signal back. Depending on the output of the comparator, the counter ramps up or down one LSB unit through DAC, so that V_{OA} tracks V_{IA} incrementally and guarantees the tracking error smaller than a half LSB finally. Fig. 1.3 shows us the signal flow of the input and DAC feedback. The essential difference of a Tracking ADC to other ADCs is that the Tracking ADC performs only one LSB data conversion during one clock cycle instead of multiple cycles. Therefore, the group delay of processing the data in the typical Tracking ADC is the shortest among the available ADCs. But the signal form of the Tracking ADC shows also the limitation of its characteristics that the Tracking ADC suffers from the slope overload.

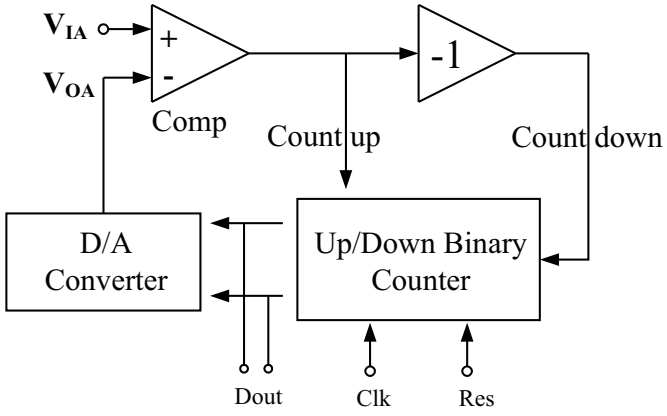

Figure 1.2: Architecture of synchronous Tracking ADC

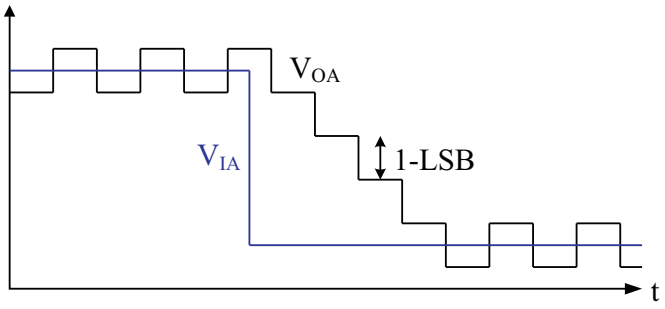

Figure 1.3: Signal flow of synchronous Tracking ADC

Fortunately, this problem does not disturb our application. According to input signal requirements this issue can be neglected by defining the Tracking ADC with the proper slew rate. The main idea behind this solution is that the output's slew rate of DC-DC converters is limited. This will be discussed further in the chapter 3.

Even if this issue of slope overload can be neglected, the traditional Tracking ADC still cannot satisfy the demand to low power consumption. Clearly the signal of disturbance has very broad bandwidth, compared to the input signal. Respecting the Shannon-Nyquist theory, the sampling rate of the traditional Tracking ADC has to be at least twice the bandwidth of disturbance signals, so as to follow the signal change simultaneously without loosing information. But this approach of sampling the signal of disturbance at high frequency leads the ADC and digital logic control in DC-DC converters to consume excessive power in the whole time frame. This characteristic constrains the application of ADCs in power management.

To employ the advantages of traditional Tracking ADC but compensating its drawback, various techniques including self-clocking and input transient detection are introduced in this work. The advantage of using these techniques in this ADC is seen in Fig. 1.4. Besides the advantage of traditional Tracking ADC that the data are converted in one clock cycle, the clock frequency in this ADC varies, depending on the slope of the input signal. It is seen that the clock frequency of ADC is at first very low, as the input signal varies slowly. But once the slope of input signal changes very fast, the clock frequency or conversion rate is increased to track the input signal with high fidelity. Based on these techniques, the trade-off issue mentioned above can be solved, because the conversion rate of this ADC is adjusted in accordance to the variation of its input signal. The working concept

of this ADC is beyond the limitation of Shannon-Nyquist theory. Thus, the mechanism of input transient detection not only guarantees the tracking fidelity but also reduces the average sampling rate, optimizing the power efficiency.

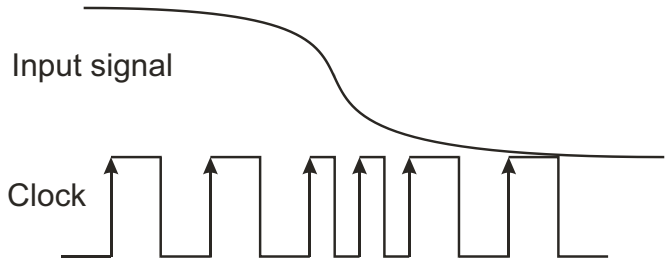

Figure 1.4: Clock flow of proposed ADC

1.3 Chapter organization

Chapter 2 presents the motivations why the system is tending to use digitally assisted analog signal. It shows the survey of performance trend for digital and analog technologies. Based on analyzing the scaling of CMOS technology, the impact on the characteristics of analog as well as digital circuit will be described, especially in terms of power efficiency for the application of power management.

Chapter 3 introduces the functional concept of the proposed ADC. It shows that this ADC achieves the best performance in terms of power dissipation and speed. To verify the new concept, the function of this ADC is modelled and simulated by ScicosLab.4.4.1.

Chapter 4 presents the characteristics of the comparator in this work. The performance of the comparator in terms of speed, resolution and noise determines the application of ADCs. By using the common-source input pair and auto-disconnection mechanism the comparator in this work not only improves the common-mode kickback noise significantly, but also reduces the differential kickback noise considerably, when compared to the traditional dynamic latched comparator. In addition, the proposed ADC requires less settling time for the signal comparison, being suitable for high-speed applications.

Chapter 5 presents the system implementation of this ADC including current mode DAC (I-DAC), counter or integarator, and digital control block. Upon the outputs of auxiliary comparators, the clock frequency of this ADC will be

self-adjusted. Furthermore, the digital control block triggers the counter that switches the I-DAC incrementally.

The evaluation and measurement of this ADC are shown in chapter 6. The characteristics about linearity and dynamic will be presented and discussed. Meanwhile, the advantages of transient-driven mechanism of this ADC will be also demonstrated.

Finally, the conclusion for this work will be summarized and some suggestions for the optimization of this ADC in the future will be also discussed.

Chapter 2

Trend to digitally assisted analog circuits

2.1 Technology evolution

Since more than three decades the semiconductor industry has achieved its impressive performance and improvement in its products as well as its research for decreasing the minimum feature sizes of the integrated circuits. This cited trend is expressed by Moore's Law. That means, in every 24 months the number of components per chip doubles [10, 11]. All of the improvements show the trend of technology evolution that is called "scaling". Enabled by large R&D investments, the chips have become cheaper, more power-efficient and faster, but also more complex.

The continuous scaling of electronics reduces the production cost of electronic components, promoting market growth for integrated circuits (IC). So it becomes meaningful for us to get the overview of the evolution of technologies and the pace of development progress. To demonstrate this trend of technology progress, DRAM or Flash memory could be chosen, because they always use the finest technology to produce the pitch with minimum dimension. Consequently, the pace of semiconductor technology evoluation are set or defined by the pitch of DRAM or flash memory, as shown in Fig. 2.1.

Referred to the documentation of [12] published by International Technology Roadmap for Semiconductors (ITRS), the roadmap of technology evolution, which is represented by the technology progress of DRAM memory, is seen in Fig. 2.2. From 2011 as a reference year a projection of 15-year time scope in the past as well as future is done and forecasted.

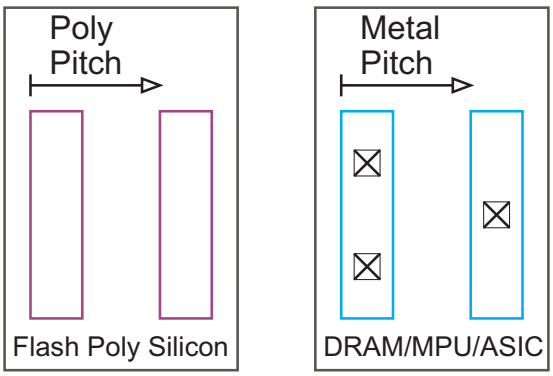

Figure 2.1: Definition of half pitch

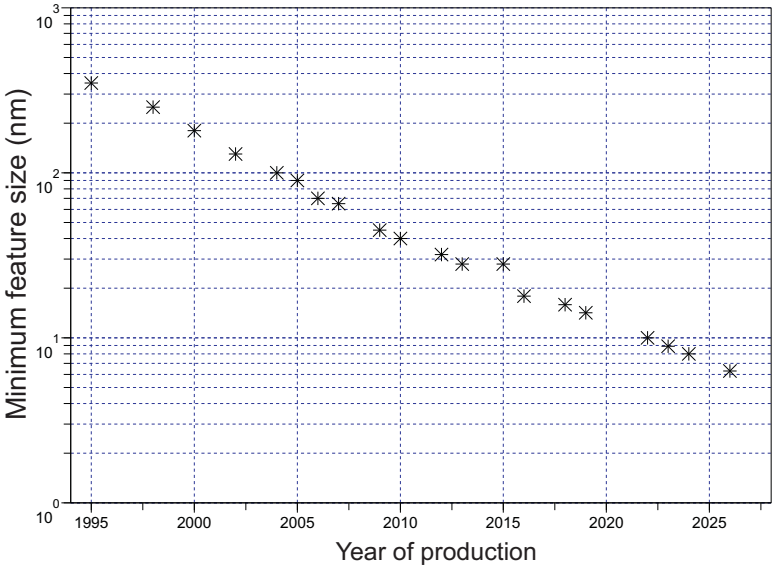

Figure 2.2: DRAM and flash memory product trend

Based on the survey from ITRS it is observed that the trend of DRAM product targets the 2.5-year technology cycle. This value is derived from the fact that the metal half-pitch of DRAM memory was 180 nm in 2000, 90 nm in 2005, and 40 nm in 2010. Afterwards, a three-year timing cycle (0.7× reduction) of DRAM metal half-pitch to 9 nm in 2024 is suggested by DRAM manufacturers.

From the above discussions and figures we can clearly see that in the next ten years, even at the beginning of 2020, the metal half-pitch will enter into the range of less than 10 nm. In other words, the minimum channel length of MOS transistor would be less than 6 nm. Even the people from the semiconductor industry feels also very hard to imagine how we could continue to promote the historic trend of technology progress in terms of costs of process equipment in

the coming 10 year.

One fact remains unchanged that most electronic devices such as microprocessors, memories, and logic devices still use silicon-based CMOS technologies, although some new applications, which are performed by passive components and sensors, do not totally scale properly with Moore's Law. But over time these functions initially fulfilled by non-CMOS technology are gradually integrated into a CMOS system on chip (SoC) within a single package or system-in-package (SiP). This trend shown in Fig. 2.3 will be further continued in vertical as well as horizontal direction [12]. The main driver for this trend combining SoC and SiP relies on data storage and digital signal processing, which are subject to CMOS technology evolution with respect to Moore's Law.

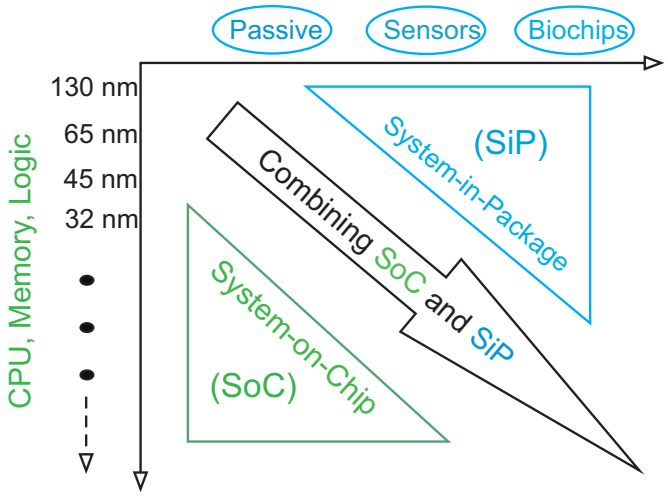

Figure 2.3: Moore's law and more

From the trend of technology evolution we can observe that no matter what kind of technology, CMOS or non-CMOS, all of them are scaled over time and integrated gradually in one system or package. The dimension of CMOS technology gets smaller and is below 6 nm in 2026, so that the systems perform faster and more power-efficient. In addition, the density of MOS transistors and other kind of component is increased.

Based on these analyses of technology evolution, many open questions are left to circuit designer: how is the effect of scaling of CMOS technology to analog and digital design? Is it the same? Should we prefer to use more digitally assisted design than pure analog? To answer these questions, the successive explorations will continue to be discussed.

2.2 Scaling analysis

In this chapter the impact of the scaling of CMOS technology on the characteristics of transistors will be investigated. By the focus on the development of CMOS technology in the past and the future the effects of the scaling of CMOS technology will be analyzed in the following sections. Meanwhile, the key characteristics of MOS transistor will be determined and demonstrated by means of the scaling of CMOS technology.

Furthermore, it should be noted that an absolute objective comparison in terms of performance of MOS transistor over time is very challengeable. Depending on the applications and the tasks, different constraints and requirements lead to different results. For this work the CMOS technology scaling shifts from generation to generation. Therefore, the comparison in this work is performed mainly according to the criterion of feature size of MOS transistor [13, 14]. The aim of this survey is mainly to illustrate the development of CMOS technology and overview the developing trend of MOS transistor, specifically which is applied in the field of power management in this work.

2.2.1 Supply voltage

With the continued scaling of CMOS technology the supply voltage shown in Fig. 2.4 is decreased to suit the increasing demand from low power applications. However, the headroom or the operational range of transistor for analog design becomes extremely critical. Low supply voltage has certainly lower headroom, resulting in reduced common-mode operational range for transistors. The number of stacked transistors in the cascode configuration has to be reduced. As a result, the high output impedance and intrinsic gain cannot be achieved. Another critical fact for analog design due to the scaling of CMOS technology is the dynamic range of circuits. As well-known, to maintain the given dynamic range the noise of circuits has to be decreased by factor of N^2, if the signal range is scaled down by factor of N. The characteristics of dynamic range are most important for high precision design and will be discussed in following section in details.

In the successive sections the comparison of MOS characteristics will be made. The technology nodes spanned in this analysis are from $0.25\,\mu$m down to 65 nm.

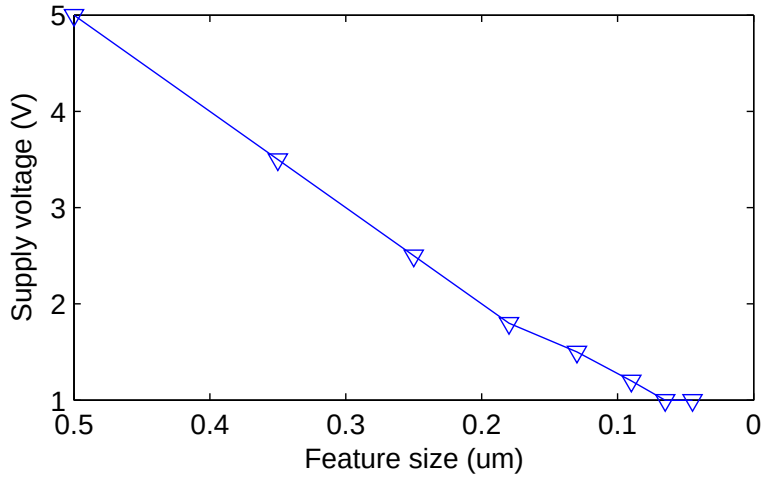

Figure 2.4: Scaling of supply voltage

2.2.2 Transconductance

The transconductance of MOS transistor quantifies the drain current change over the gate voltage [15, 16]. Different formulas have been used in Eq. 2.1 to express its characteristics, which are valid to NMOS as well as PMOS transistor. The transconductance of the MOS transistor is

$$g_m = K_P \cdot \frac{W}{L} \cdot (V_{gs} - V_{TH}) = \sqrt{2 \cdot K_P \cdot \frac{W}{L} \cdot I}, \; where \; K_P = \mu_{n/p} \cdot C'_{ox} \quad (2.1)$$

where K_P, $\mu_{n/p}$ and C'_{ox} are the coefficient of process technology, the charge mobility and the oxide capacitance per area.

Assumed that the NMOS transistor has a minimum size and the overdrive voltage of $V_{gs} - V_{TH}$ is constant. So the transconductance is mainly dependent on the process parameters, which include the carrier mobility and the oxide capacitance per area. The oxide capacitance per area in the MOS field is defined as:

$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \quad (2.2)$$

where the dielectric is constant, but the thickness of gate dielectric denoted as t_{ox} is scaled down. In the long-channel modeling, it is alway assumed that the carrier mobility is kept constant. But with the scaling of MOS technology it is not the case. Many contributions have been made, attempting to explain the characteristics of carrier mobility. Generally it can be said that in the reality the mobility is reduced due to highly doped channel region and the associated

scattering mechanisms. And the mobility of carrier is inversely proportional to the dopant concentration roughly and approximately [17, 18, 19, 20].

$$\mu_n \sim \frac{1}{N_D}$$

The dopant concentration is scaled up, whereas the thickness of gate oxide is scaled down. Both parameters compensate each other and keep the coefficient of process technology K_P constant with the MOS scaling. Therefore, the trend of transconductance should remain constant or comparable. Fig. 2.5 shows the experimental data of MOS transconductance [13]. The variation of MOS transconductance over the scaling of feature size is very limited and comparable from 84 μS to 96 μS.

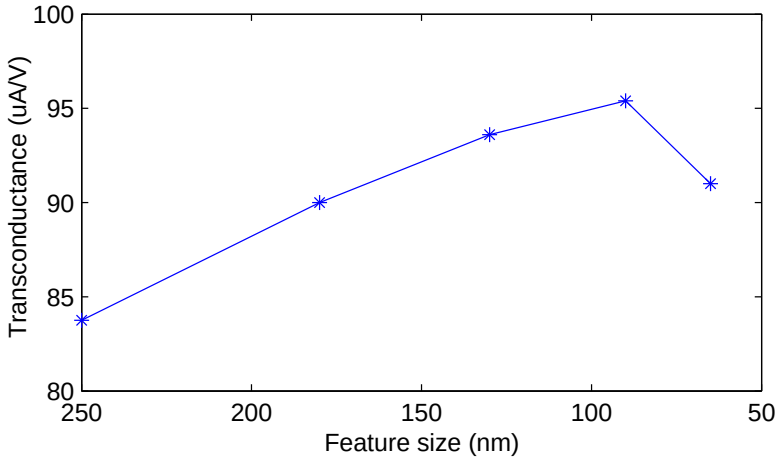

Figure 2.5: Scaling of transconductance

2.2.3 Intrinsic gain

The result that the transconductances of the scaled MOS transistors are within the same order, may be disputable. However, when the intrinsic gain of MOS transistor is considered here, the change of transductances of MOS transistor over scaling becomes reasonable.

The intrinsic gain of MOS transistor is defined as the product of the transconductance and output resistance as Eq. 2.3:

$$A = g_m \cdot r_o, \ where \ r_o \ \sim \ L \tag{2.3}$$

When the transconductances of different process technologies with scaling are approximately equal, the intrinsic gain will decrease as expected in Fig. 2.6, because the output resistance is reduced with the scaling. However, for high precision circuit this result challenges the circuit design. Especially for the feedback loop without high gain, the linearity of circuit is harder to achieve. One possible solution for this problem is to use cascode transistor in stack to boost the output impedance and gain. Yet the reduced signal swing range mentioned in above section constrains the utility of this approach. Therefore, this approach can only be made, depending on the application and associated conditions.

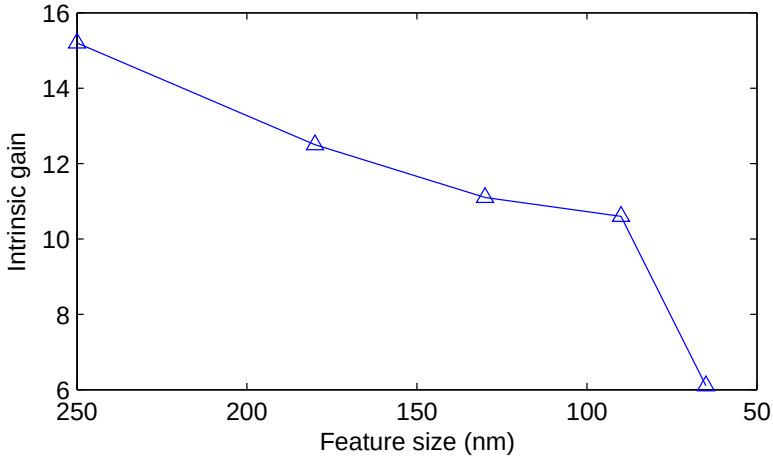

Figure 2.6: Intrinsic gain scaling

2.2.4 Transit frequency

The transit frequency is derived from small signal model and is considered as the frequency, where the current gain of MOS transistor is equal to one, as defined in Eq. 2.4 from [21].

$$\frac{\partial i_d}{\partial i_g} = \frac{g_m}{2 \cdot \pi (C_{gs} + C_{gd})} \tag{2.4}$$

Due to $C_{gs} \gg C_{gd}$ the transit frequency can be rewritten as Eq. 2.5. Hence for the given overdrive voltage we can observe that the transit frequency is mainly determined by its channel length or minimum feature size.

$$f_T \approx \frac{g_m}{2\pi C_{gs}} = \frac{3K_P(V_{gs} - V_{TH})}{4\pi L^2 C'_{ox}} = \frac{3\mu_n}{4\pi} \cdot \frac{V_{DS,sat}}{L^2} \tag{2.5}$$

$$f_T \propto \frac{1}{L} \; (Short - channel\; modeling) \tag{2.6}$$

However for the transistor using the minimum feature size, the electron mobility is not constant and decreases as the electron reaches its saturation-velocity. Approximately the transit frequency is inversely proportional to the channel length as Eq. 2.6. The data of NMOS transit frequency for minimum dimension in diverse technologies for the given overdriven voltage are shown in Fig. 2.7.

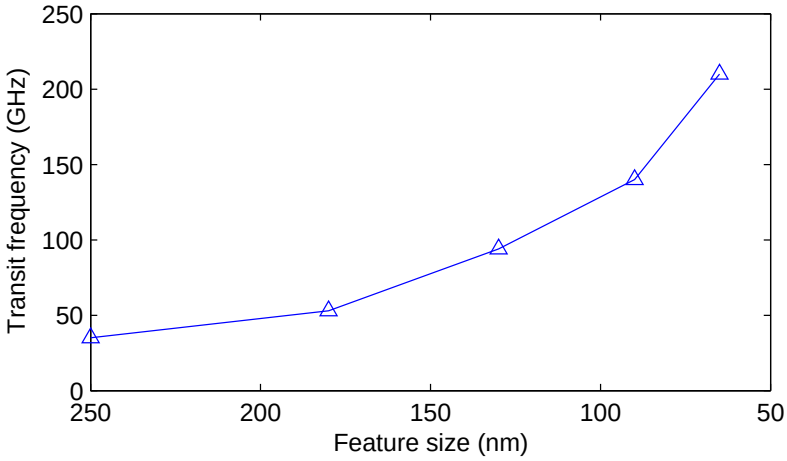

Figure 2.7: Scaling of tranconductance scaling

The characteristics of transit frequency have fundamental important meaning for high speed application, because the bandwidth of signal is determined by the transit frequency. Therefore, to achieve the high speed only the devices with minimum size should be used.

2.2.5 Transistor dynamic range

The dynamic range of MOS transistor is determined by the ratio of the signal range to the noise. For MOS transistor two significant noise sources disturb the behavior of circuits. The flicker noise, also called 1/f noise, is generated by trapping or de-trapping electrons at the oxide interface. Eq. 2.7 indicates the power spectral density (PSD) [22]:

$$V_{flicker}^2 = \frac{K_f}{C_{ox}WL} \cdot \frac{1}{f} \tag{2.7}$$

where K_f is process parameter. Inserting Eq. 2.2 into Eq. 2.7, the PSD of flicker noise is equal to:

$$V_{flicker}^2 = \frac{K_f}{C_{ox} \cdot WL \cdot f} = \frac{K_f}{C'_{ox} \cdot W^2L^2 \cdot f} \tag{2.8}$$

Although the C'_{ox} is increased with CMOS scaling, the scaled minimal channel length and width decrease the denominator of Eq. 2.8. Therefore, the PSD of flicker noise is increased with the scaling of MOS transistor. Consequently, the flicker noise for the low bandwidth circuits is increased. However, in the wideband application, which is introduced in chapter 4, the flicker noise has minor value and could be neglected.

The thermal noise of MOS transistor for wide-band applications is very critical and serious [23, 24]. The dynamic metric of MOS transistor get even worse.

We assume that the signal swing is defined as supply voltage, and the parameters of γ and Δf described in Eq. 2.9, are set to 2/3 and 1 respectively to demonstrate the comparison of noise characteristics. The input-referred noise voltage is inversely proportional to g_m, as written in Eq. 2.10. But the g_m of MOS transistor is not scaled proportionally with technology scaling. The variation of g_m in different technologies is very limited and comparable, while the supply voltage is scaled properly. Therefore, the dynamic range of smaller technologies shown in Fig. 2.8 is reduced and becomes more critical for analog circuit design.

$$i_d^2 = \frac{2}{3} \cdot 4k_B T \cdot g_m \cdot \Delta f \tag{2.9}$$

$$v_g^2 = i_d^2 \cdot \frac{1}{g_m^2} = \frac{8k_B T \cdot \Delta f}{3g_m} \propto \frac{8k_B T}{3g_m},\ where\, \Delta f = 1\, Hz \tag{2.10}$$

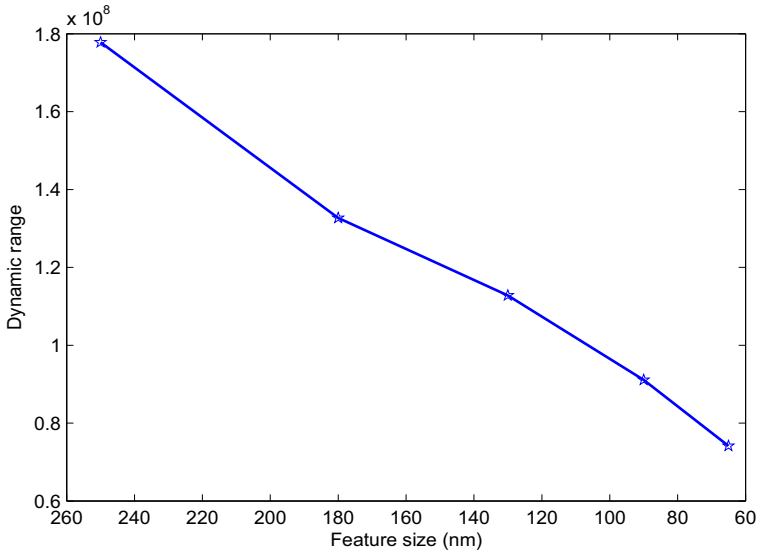

Figure 2.8: Scaling of dynamic range

2.2.6 Transistor mismatch

Process variation by production of two adjacent identical MOS transistors causes the mismatch. For certain applications, which require high precise characteristics of MOS transistor, the mismatch can become the bottleneck and limits the performance of circuits.

The most cited definition to describe the deviation by means of parameter P is introduced in [25]:

$$\sigma\left(\Delta P\right) = \frac{A_P^2}{W \cdot L} + S_P^2 \cdot D^2 \tag{2.11}$$

Where A_P is area proportionality constant for parameter P, where S_P describes the variation of parameter P for different positions and coordinates on the wafer [25]. By using Eq. 2.11, the mismatching factor due to the deviation of V_{TH} and β for drain current of MOS transistor could be derived as:

$$var\left(\Delta V_{TH}\right) \cong \frac{A_{VTH}^2}{W \cdot L} \tag{2.12}$$

$$var\left(\Delta \beta\right) \cong \frac{A_{\beta}^2}{W \cdot L} \tag{2.13}$$

In NMOS transistors the gate voltage minus the threshold voltage ($V_{gs} - V_{TH}$) over the oxide creates the inversion layer and the depletion region. The threshold voltage is dependent on the thickness of dielectric and the bulk doping. Consequently, the mismatching due to the threshold voltage is determined by the deviation of gate dielectric thickness and the doping fluctuation. With the development of technology scaling, the better control of implantation and diffusion would improve the parameter of area proportionality.

The data shown in Fig. 2.9 [26, 27] illustrate the trend of parameters of A_{VTH} and A_β for the seven generation technologies from 2.5 μm down to 65 nm. The parameter of A_{VTH} with technology scaling is improved, and the parameter of A_β is also improved, but the scope is very constrained and can be considered as constant.

2.2.7 Power efficiency

The power efficiency of MOS transistor represents the performance of MOS transistor for " energy per operation". This description will illustrate how efficient the MOS transistor can be operated at a certain speed.

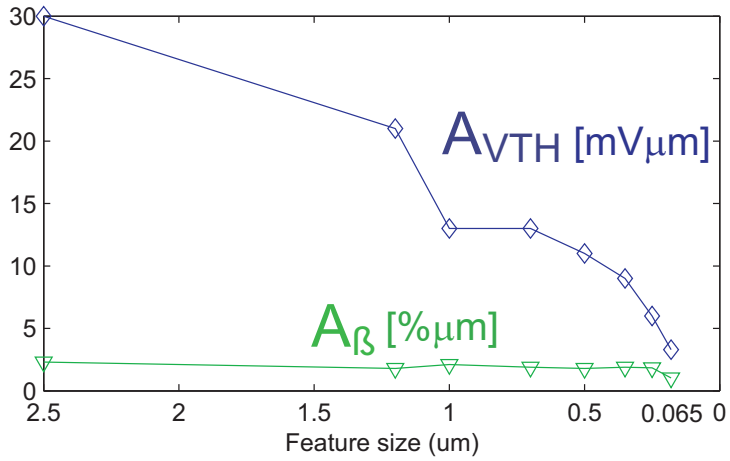

Figure 2.9: Scaling of MOS transistor mismatching

The common figure of merit (FOM) is used to describe this characteristics of ADCs [28] and is defined by Eq. 2.14:

$$FOM = \frac{P}{f_T \cdot 2^{ENOB}} \tag{2.14}$$

Where f_T is the transit frequency and ENOB represents the effective number of bits. P is the power consumption of the ADC. Eq. 2.14 can be also applied in this case to MOS transistors for the comparison of power efficiency.

However, ENOB depends on the signal to noise and distortion ratio (SNDR), which is defined at the maximum Nyquist frequency that the ADC can achieve. As mentioned above, with the scaling of CMOS technology the noise of MOS transistor is not scaled properly and the SNDR gets worse. But it is also proven that the CMOS technology scaling improves the cost-efficiency and increase the MOS transistor number density. Based on the given analysis, we perform the comparison by deriving Eq. 2.14 to:

$$FOM = \left.\frac{Power}{Speed}\right|_{ENOB=const} \tag{2.15}$$

under the assumption that the ENOB is given and constant.

Maybe some readers are confused by such assumptions that apparently the SNDR deteriorates the ENOB of ADCs with technology scaling. Consequently the FOM should be degraded. But the aim of the comparison in this section is just to emphasize how efficiently the MOS transistor in ADCs can operate at a given ENOB, where the SNDR still satisfies the applications.

Besides the cost-efficiency of CMOS production, this result derived from the comparison is absolutely the major driver of CMOS scaling technology, as shown in Fig. 2.10 [13].

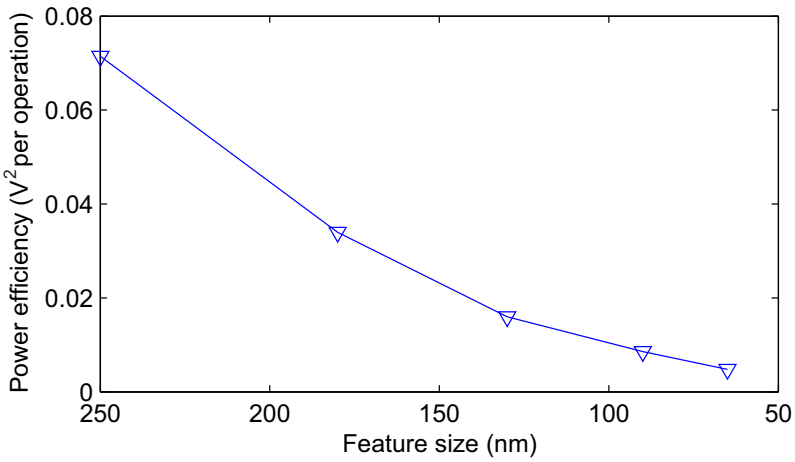

Figure 2.10: Scaling of power efficiency

2.3 Digitally assisted mixed signal system

In this section we will specifically discuss the surveys performed in section 2.2 and try to explain why systems used in most applications will become more digitally assisted mixed signal system instead of pure analog. Furthermore, we also want to show what kind of new contributions the digitally assisted mixed signal system can make to the applications of semiconductor industry, especially for power management, while fitting the development of CMOS technology.

Obviously, different criteria lead to different consequents and results, if the performances of diverse systems and concepts are compared. Throughout this work the concept of power efficiency will be considered as a fundamental, because the increasing demand on battery powered devices become a new highlight and enhances the shift of the criteria to be more power-efficient orientation.

2.3.1 Performance gap between digital and analog circuits

The ITRS road map shows that the feature size of MOS transistor will be further reduced, and the density of CMOS transistors in a single chip is increased to enhance the functionalities and applications. On the other hand the CMOS

scaling affects the performance of digital and analog circuits. Although different applications have diverse constraints and requirements, the general but also the fundamental desire that we expect from the circuits is that the circuit can perform at high speed, while dissipating low power. In other words, we want to achieve the maximum power efficiency in any application.

In section 2.2 the key characteristics of MOS transistor with the scaling have been discussed and analyzed. Deepening into the key characteristics of MOS transistor demonstrated above, it is obvious that not all of them are important and crucial for the applications of analog and digital circuits at the same time. Therefore, it is important to discuss the challenges of analog as well as digital circuit design, respectively.

2.3.1.1 Analog design challenges

Principally the characteristics of analog circuits are limited by electronic noise, speed and power consumption [29]. Scaling of CMOS technology improves the performance of analog circuits only conditionally. Unlike in digital logic the analog transistors must resolve and amplify extremely small signal.

Fig. 2.11 shows the relationship between speed and accuracy requirements regarding power dissipations [29]. The accuracy of the circuits depends on noise, matching and linearity. The most critical factor for analog circuits belongs to the thermal noise. The trivial solution for reducing the thermal noise in circuits is cooling, because the thermal noise is dependent on the absolute temperature (Kelvin). However, this method is not suitable and practical for the most applications. The second approach for this issue is to use MOS transistors with large g_m. But a MOS transistor with large g_m consumes also a lot of current. Besides that, in switched capacitor circuits the noise can be reduced by increasing the switched capacitance. More precisely, if we want to reduce the noise by a factor of two, the increase of the effective capacitance has to be quadrupled.

$$V_{total\_n} = \sqrt{\frac{k_B T}{C}} \tag{2.16}$$

Under the condition that the charge or discharge speed remains constant, this results in a fourfold increase in transconductance and hence a fourfold increase in current and power dissipation, as indicated in Eq. 2.17:

$$g_m = \frac{2I_{DS}}{V_{gs} - V_{TH}} \tag{2.17}$$

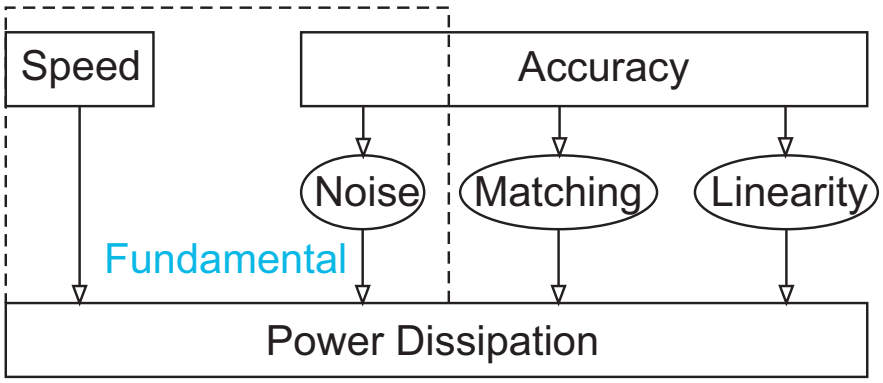

Figure 2.11: Analog circuit design trade-off

The second limitation due to scaling of CMOS technology is mismatching. Eq. 2.12 and Eq. 2.13 express clearly that the matching characteristics of components are inversely proportional to its feature size or area. One simple approach for solving this issue is to increase the area of MOS transistors, resulting in large capacitances. Under large signal operation these capacitances would require a high static current.

In addition to mismatch, high linearity of the analog circuit and feedback loop is also affected by CMOS scaling. The analog circuits achieve high linearity by using the operational amplifier with high gain. But due to the scaling, the gain of single MOS transistor is reduced as seen in Fig. 2.6. The use of cascode structures in operational amplifier can improve the output impedance and the intrinsic gain, but the reduced supply voltage constrains the signal head room of the cascade transistors. Therefore, multistage operational amplifier become the alternative to increase the gain, but this results in additional power dissipations and makes frequency compensation more challengeable.

In contrast to noise disturbance, mismatch and linearity are not the fundamental issues. Mismatch and linearity error can be reduced by modifying the local transistors dimension without dissipating additional power. At the system level, these constrains could be solved by the use of trimming [30, 31, 32] or calibration digitally [33]. These approaches achieve great performance and the characteristics of matching and accuracy are improved significantly. Therefore, the issues of mismatching and linearity have secondary priority.

Many research works have made great contributions to the reduction of noise disturbance. But the most of them focus on the flicker noise, or 1/f noise, which

appears only in the low frequency range. Based on these characteristics of flicker noise, chopper and correlated double sampling (CDS) techniques are explored to reduce the flicker noise significantly by a factor of more than 100 [34, 35, 36]. The thermal noise seems to be more difficult to be addressed due to the wide bandwidth. Oversampling techniques can reduce the thermal noise power density [37], improving the noise characteristics of circuits for the given bandwidth of signal. However, these techniques dissipate unfortunately high power, because to reduce the thermal noise about factor of two, the oversampling rate has to be increased by same factor of four. This leads to very high dynamic power dissipation, proportional to the sampling rate.

2.3.1.2 Digital design challenge

The digital circuit design benefits definitely from CMOS scaling. Compared with analog design, the digital circuits are driven by the logic levels, charging or discharging the load capacitance at the output of digital circuits to the supply voltages. So the characteristics of analog circuits, also referred to noise, mismatching and linearity, are not very sensitive in the application. According to the same criterion of power efficiency, we can clearly observe that the digital circuit design with CMOS technology scaling dissipates lower power, while being able to achieve higher speed. The power dissipation of digital circuits described by Eq. 2.18 is determined by the supply voltage. So the power dissipation is reduced by the scaling of supply voltages.

$$P = C_{Load} \cdot V_{DD}^2 \cdot f \tag{2.18}$$

Furthermore, the transit frequency of MOS transistor is also increased with the scaling of CMOS technology. This property enables the digital circuits to achieve higher clock rates for high speed applications.

Based on the discussion and analysis above, the impact of CMOS technology scaling on analog as well as digital circuit is summarized in Table 2.1. It shows the direction that the characteristics of MOS transistor develop, along with the scaling of CMOS technology. The key parameters of transconductance, intrinsic gain, dynamic range and mismatching show a negative trend, whereas the characteristics for digital applications illustrated by parameters of supply voltage and transit frequency are improved by CMOS scaling.

Table 2.1: Scaling effects for digital and analog design

	Supply Voltage	Gm	Gain	f_T
Digital	+	*	*	+
Analog	−	−	−	+
	Dynamic Range	Mismatch	Power Efficiency	
Digital	*	*	+	
Analog	−	−	+	
"+": positive trend; "−": negative trend; "*": do not care				

So far, we have analyzed the trend of technology development and impacts of CMOS scaling on analog and digital circuits. Over time it will become more apparent that the beneficial gap between digital and analog circuits will be further enhanced. Especially for analog circuits the performance will be constrained by the scaling of CMOS technology. But the world is analog, and analog circuits are indispensable for analog signal. Therefore, to combine the advantages of digital and analog circuits, the circuit designer tend to choose more digitally assisted circuits.

For most applications Fig. 2.12 shows a general approach of the signal flows between real world and the system. It is shown in part (a) that the signal is digitized directly after filtering the disturbance signal from real world, so that the number of analog circuits could be reduced conditionally. The associated limitation caused by analog parts due to technology scaling and the operational environment thereby is partially optimized.

Different approaches have been developed to improve the signal processing by digital systems, while improving the power efficiency. One of them shown in part (b) of Fig. 2.12 [29] introduces digital postprocessing to calibrate the system error. This approach relaxes the limitations, which imposes analog circuit design due to CMOS scaling. The drawback is that the algorithm of digital postprocessing becomes more complex. But all of these methods principally share the common aim that with respect to the performance of ADC the power efficiency can be optimized and improved. In other words, the driving force of these approaches is to pursue the maximum power efficiency of the ADC, as well as for the whole systems.

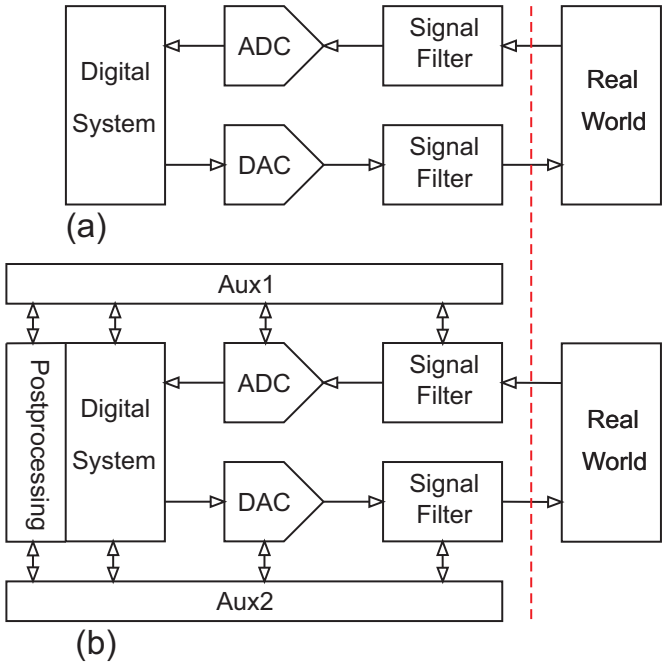

Figure 2.12: Signal processing system and interface

2.3.2 Power efficiency of ADCs

Since the introduction of semiconductor technology, there is huge number of ADCs available to be utilized in the modern SoC. Regarding the structures and operation algorithms, the ADCs consist of two categories generally, which are Nyquist ADCs and Oversampling ADCs. Depending on constraints and requirements of different applications in the industry, the ADCs with different architectures often need to be selected specifically to satisfy the specifications. In this section the features of ADCs in terms of power dissipation, speed and efficiency will be discussed in detail, as to familiarize with the background and to achieve the overview.

Oversampling ADCs as Sigma-Delta ADCs are very popular for many industrial applications, which require high resolutions. Oversampling ADCs principally are operated by the combination of two signal processing techniques, which are oversampling and noise shaping [38]. One of main errors causing the degradation of the performance of Oversampling ADC is due to quantization errors. Through oversampling techniques, PSD of quantization error is distributed in the larger frequency band by oversampling, which results in lower PSD of quantization error. Thus, the resulting and integrated noise in the band-limited frequency range

is reduced. Along with oversampling techniques, noise shaping techniques will further reduce the quantization noise. In the way of filtering the quantization noise, the main part of quantization noise is reshaped far away outside the band-limited signal. Based on the combination of both techniques, the resolution of oversampling ADC could reach values beyond 16 bits, as shown in Fig. 2.13 [39].

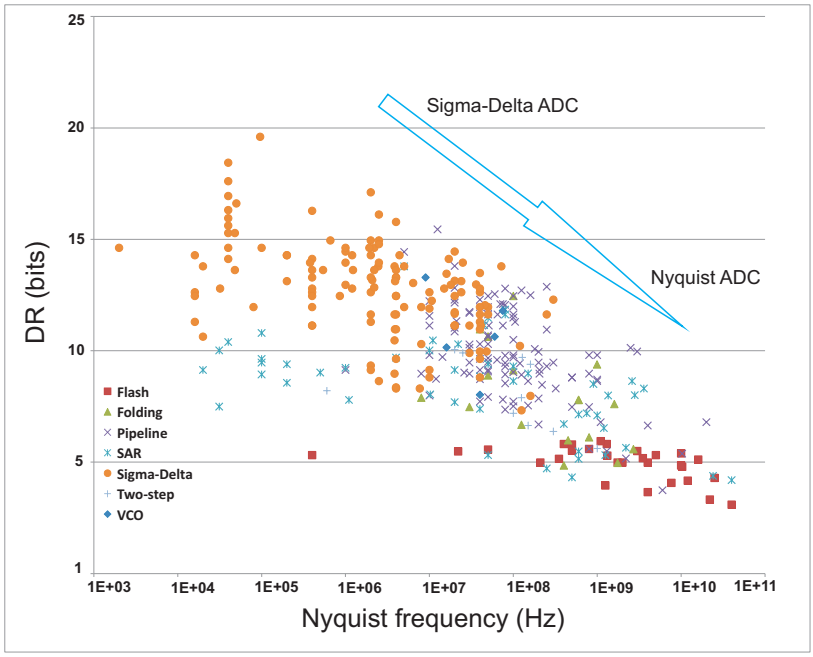

Figure 2.13: DR versus Nyquist frequency

However, the Oversampling ADCs have also limitations, which are caused unfortunately by oversampling and noise shaping techniques themselves. To decrease the quantization noise by a factor of oversampling ratio (OSR), which is defined as the ratio of oversampling frequency to Nyquist frequency of the input signal, the OSR is normally set to be 32...256, for example. So the dynamic power dissipation, which is proportional to the sampling frequency, is considerably high. Noise shaping techniques push the main part of quantization noise far away from the input signal bandwidth, yet the successive decimation filtering of the noise outside the signal bandwidth produces a long group delay and also consumes enormous power. Hence, the Oversampling ADCs are not suitable for applications that need small and medium resolutions, but require high conversion rate and low power consumption.

Totally different to the Oversampling ADCs, the Nyquist ADCs operate the data conversion by means of exploring the signal binary over the full scale. The input signal needs to be sampled at the Nyquist frequency, which is twice of input signal bandwidth instead of oversampling frequency. So the power dissipation and conversion rate of Nyquist ADCs are lower and faster than their counterpart in general. However, for the Nyquist ADCs it is difficult to achieve high resolution. This is due to the quantization errors, which can not be reshaped and filtered as in Oversampling ADCs. Therefore, the topology of Nyquist ADCs becomes dominant for resolutions up to 12 bits and conversion rates of maximum 2 GS per second. Such applications include e.g. data compression and wireless transceiver.

The power efficiency of ADCs needs to be further improved. By performing the first-order estimation of power and conversion speed of Nyquist ADCs the best entry point for this aim is identified [40]. Fig. 2.14 shows at first the four mostly used Nyquist ADC topologies, which are Flash, Pipeline, SAR and Tracking ADCs. Traditionally, Flash ADC is in the favor of high speed application [41, 42, 43]. For N-bit converter, $2^N - 1$ comparators are parallel connected with the entire quantization levels to perform the operation just in one clock cycle. The decoder converts the thermometer codes to binary codes, dissipating also extra power. Because the main part of power dissipation is caused by dynamic switched comparators, the total power consumption of a Flash ADC is roughly considered as 2^N. Regarding the fact that the conversion is done and completed within one clock cycle, the speed or conversion rate of Flash ADC is normalized to 1. Instead of accomplishing the data conversion within one clock cycle, Pipeline ADC [6, 5] uses several stages to perform the conversion, and the number of stages is proportional to the number of bits. The advantage of this topology over Flash ADC is that the exponential number of comparators is reduced to the number of bits. Therefore, the total power dissipation is enormously reduced. Furthermore, in the inter-stage the residue amplifier is needed which consumes high power and limits high-speed operation by its bandwidth. Thus, we would like to say that the total power dissipation is larger than N with the conversion rate less than 1. SAR ADC also uses several stages to convert the input signal and is operated in the way similar to Pipeline ADCs. The difference between them is that instead of processing the data in parallel as in Pipeline ADCs, the SAR ADCs execute the binary search sequentially. The advantage of this approach for N-bit SAR ADCs is to use only one comparator to accomplish the data conversion but at

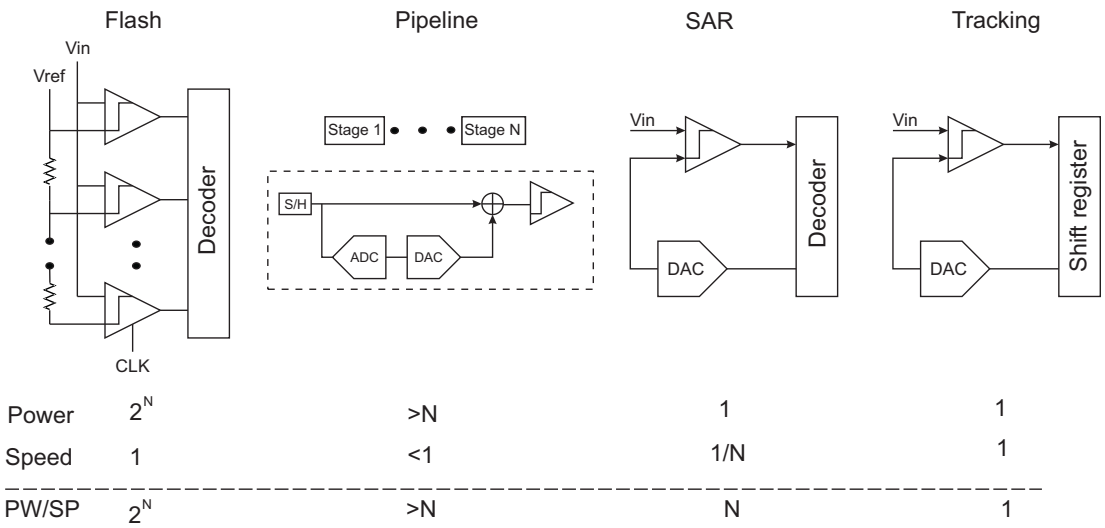

Figure 2.14: Conventional architectures of Nyquist ADCs

the expense of N clock cycles. Hence, the power consumption is simplified as 1 approximately, while the conversion is equal to 1/N.

Delta-encoded or Tracking ADC performs similar to SAR ADC, except that the SAR ADCs execute the binary search over the full scale range, whereas the Tracking ADC processes only one least bit (LSB) per conversion within one clock cycle. The Tracking ADC achieves the shortest group delay and utilizes also only one comparator. Therefore, the power dissipation, as well as the conversion rate, is normalized to 1.

Since the ratio of power dissipation and conversion rate presents the characteristics of power efficiency, it is well seen that the SAR ADCs have the clear advantages in terms of power efficiency over all of the other ADCs if the full scale range is searched, as shown in Fig. 2.15. But in practical applications the input signal of ADCs does not always swing from rail to rail voltages like unit-step signal. Especially for the application in power management the output signal of DC-DC converter swings only with limited slew rate, so the ADCs with the traditional binary search become unnecessary and consume lot of useless power. In this case, the Tracking ADC promises an optimal starting point for the application in power management to achieve the maximum power efficiency as shown in Fig. 2.14.

After discussion and illustration of features of ADCs we summarize a brief conclusion and emphasize that the Oversampling ADCs are in the favor of high resolutions instead of low power and high speed applications. If the binary search

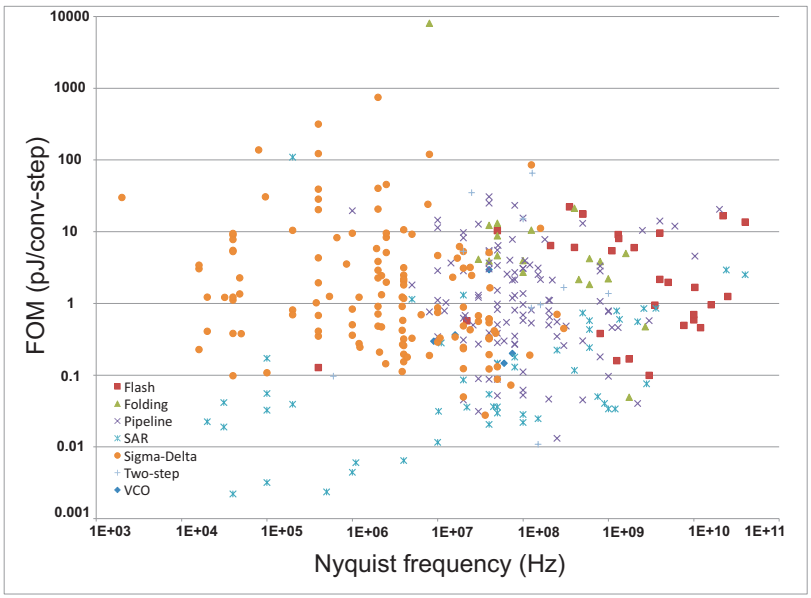

Figure 2.15: FOM versus Nyquist frequency

over full signal range is required, SAR demonstrates the power-efficient advantages over the other Nyquist ADCs as Flash and Pipeline ADCs. But for specific applications in the field of power management the SAR ADCs are not an optimal solutions, because Tracking ADCs can increase further the power efficiency and the conversion rate, suiting the signal features of DC-DC converters.

2.4 Digital control vs. Analog control of power management

DC-DC converters convert the input voltage to the output with different voltage level. The conversion is implemented by using reactive storage components, e.g., inductor and capacitor, to improve the efficiency. Meanwhile, to keep the output voltage stable, control loops are integrated in DC-DC converters. However, due to the scaling of CMOS technology the pure analog controllers encounter increasing challenges because of noise and process variation, which results in diminished dynamic range. Consequently, the digitally assisted DC-DC converter becomes more popular. In this section analog and digital controllers will be introduced and discussed to provide the reader an overview of their features.

A typical switching power converter as buck converter is shown in Fig. 2.16. The controller regulates the output voltage of DC-DC converters by using a neg-

ative feedback loop in principle. In the voltage mode the analog controller senses the scaled output voltage and compares it with the defined reference voltage. Then the error voltage is amplified to adjust the duty of the pulse width in the pulse width modulator (PWM). Depending on the duty ratio of PWM, the energy from the power supply is fed to the filter comprising the reactive components of inductor and capacitor. The filter stores and converts the energy losslessly, so that the averaged value equal to the desired output voltage appears at the output of DC-DC converters.

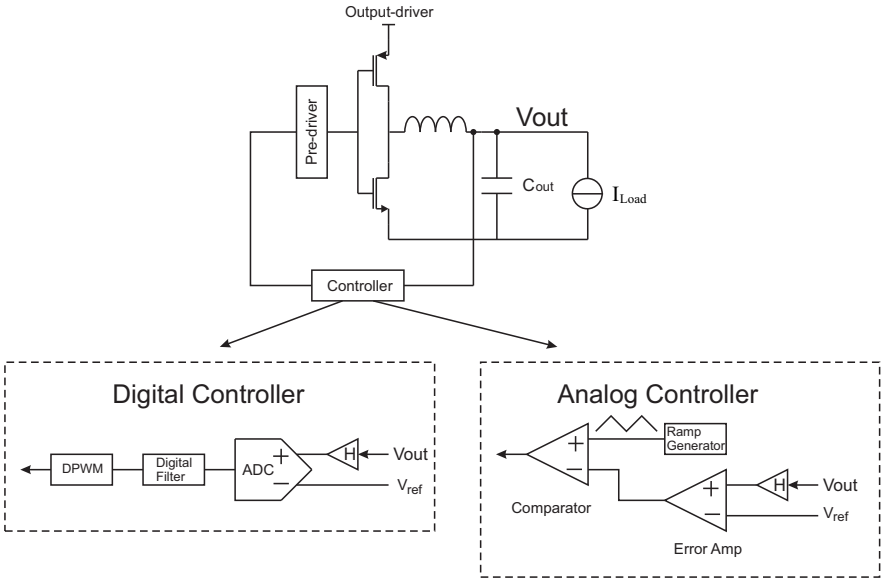

Figure 2.16: Comparison of analog and digital control

Since the controller is in the feedback loop, the issue of stability in the closed loop must be addressed. For the closed loop a phase margin of greater than 60° is required. Therefore, we consider the transfer function of the filter indicated in Eq. 2.19

$$\frac{V_{out}}{V_{in}} = \frac{1}{s^2 \cdot LC_{out} + s \cdot \frac{L}{R} + 1} \tag{2.19}$$

where V_{in} is the output of Output-driver, additionally L, C_{out} and the output load resistance R are defined to be $1\,\mu$H, $20\,\mu$F and $2\,\Omega$, respectively.

It is found that the reactive components in the second order filter have occupied the entire available phase margin, as shown in Fig. 2.17. So the delay introduced by the controller in the feedback loop would bring the system in the state of instability. Therefore, the compensation of phase margin must be inte-

grated into the error amplifier to make sure that the circuit is stable under the required conditions.

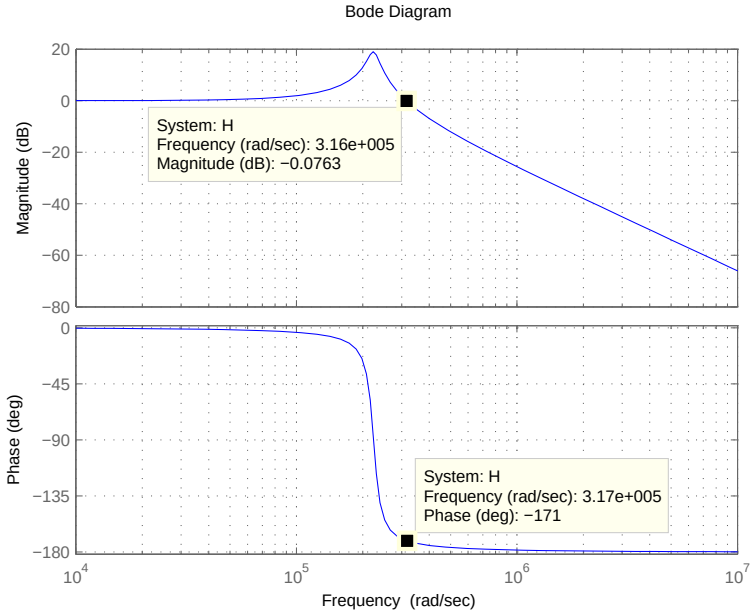

Figure 2.17: DC-DC output transfer function

It is also possible that the same loop transfer function realized in the analog system is implemented in the digital control. The digital controller works actually equivalent to the analog controller. Instead of the error amplifier, the ADC samples the error voltage and provides it digitally to the successive digital filter or PID. The task of digital filter is to guarantee the stability of the feedback system by calculating and processing the digital signal. Upon the data stream from the digital filter, DPWM adjusts the duty of the pulse width to achieve the expected output voltage as the analog controller does.

Commonly the digital filter is realized as PID controller. The output voltage translated into digital words by the ADC is calculated and processed by the PID control block in accordance to Eq. 2.20 similarly

$$U_{(z)} = \left[K_p + \frac{K_i}{1 - z^{-1}} + K_d \cdot \left(1 - z^{-1}\right) \right] \cdot E_{(z)} \tag{2.20}$$

where K_p, K_i and K_d represent the coefficients of proportional, integral and derivative constants of the controller, respectively. $U_{(z)}$ is the command of PID to

DPWM. After rearrangement, the equation can be rewritten as Eq. 2.21:

$$\begin{aligned} U_{(z)} &= U_{(z)} \cdot z^{-1} + \left[K_1 + K_2 \cdot z^{-1} + K_3 \cdot z^{-2}\right] \cdot E_{(z)} \\ and\ K_1 &= K_p + K_i + K_d \\ K_2 &= -K_p - 2K_d \\ K_3 &= K_d \end{aligned} \tag{2.21}$$

The coefficients of PID determine the frequency response of the closed loop and ensure that the control system works stable. Meanwhile, the tunable coefficients demonstrate us one of the most powerful aspect of digitally assisted power management that the coefficients can be stored in the registers and can be modified "on-the-fly", if required. Unlike the analog controller, in which the characteristics of the frequency response are already fixed by the produced silicon, the reusable IP could be precisely configurated to adapt to overall dynamic response of converters. Thus, the digitally assisted system is not only easy to be configurated, but also robust against the process variation and the disturbance from the related working conditions.

A suitable ADC for the application of power management to design remains still the challenge for designer, because the PID in digital control system relies on the data stream provided by the ADC. Only accurate processing of the error signal by the ADC can result in proper voltage at the output of DC-DC converter. Also the power dissipation of the ADC is critical, because a 6-bit ADC with 400 KS/s can consume even the power of tens of mW [44], which is too much for digital DC-DC converters in mobile electronics. In addition to the power dissipation of the ADC, the group delay or "dead time" is very crucial, because long group delay leads the converter to be unstable. Given the fact above, we can say that the design of low resolution ADC with low power but high speed is the key aim in this work.

Before finishing this section, let us summarize and list the characteristics of digitally assisted control system as:

Positive		Negative	
✓	Robust against processs deviation	×	High power dissipation of ADC
✓	Inherent noise immunity		and digital control logic
✓	Flexible "on-the-fly" configuration	×	Low speed of ADC

Chapter 3

Principle of proposed ADC

The characteristics of ADCs as interface circuits in digitally assisted DC-DC converters play a dominant role and determine the performance of DC-DC converters. However, due to the constrains and limitations of digitally assisted DC-DC converters, the design of an optimal ADC for DC-DC converters has special requirements. Therefore, the new concept of current-mode delta-encoded ADC with transient-driven self-clocking for digitally assisted DC-DC converters is introduced, explained and discussed in this chapter.

3.1 Architecture

3.1.1 Current-mode tracking ADC

The performance of DC-DC converters depends on the characteristics of power conversion efficiency. So the power dissipation of ADCs in digitally assisted DC-DC converters should be as low as possible. Meanwhile, to ensure that DC-DC converters work stable, even the disturbance occurs, the "dead time" of feedback control system, which is determined by the group delay of ADCs and filters, should be as short as possible. Otherwise, the control feedback in DC-DC converters cannot follow the signal variation simultaneously. If both requirements of DC-DC converter are considered at the same time, they can be derived that the high power-efficient ADCs are required for the application in digitally assisted DC-DC converters.

As mentioned in the last section, SAR ADCs have the advantages to the other kinds of ADCs. They achieve the best result in terms of power efficiency, if the binary search over the whole operation scope of ADCs is necessary. Tracking ADC

further improves the power efficiency, based on the operation mechanism similar to SAR ADCs. The only difference between them is that the Tracking ADC processes single LSB of data conversion during one clock cycle, but produces also the shortest group delay. Therefore, we can say that under the specific conditions and features, the Tracking ADC could bring the systems the most advantages among the available ADCs.

To verify the possibility of application of Tracking ADC, the output voltage characteristics of DC-DC converters are analyzed. In Fig. 3.1 one buck converter with the output capacitance (C_{out}) of 20 μF is assumed to be driven at 1 MHz per switching clock (f_{SWITCH}). In the case of the load step, the maximum load current is increased about 1 A ($\Delta I_{Load} = 1$ A) at the output of DC-DC converter, the current is drawn from the capacitor and the inductor to supply the output load. If in the worst case the current is only provided by the load capacitor, the maximum slew rate (SR) of the output voltage is derived from Eq. 3.1:

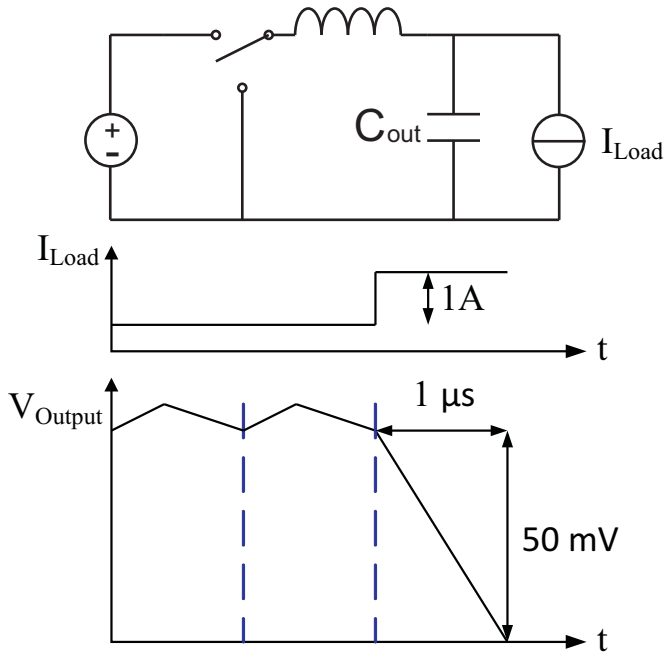

Figure 3.1: Slew rate of voltage in a DC-DC converters. With an output capacitance of 20 μF and a load current step of 1 A the maximum voltage slope is 50 mV in 1 μs.

$$I = C \cdot \frac{\partial V}{\partial t} \Rightarrow \frac{\partial V}{\partial t} = \frac{I}{C_{out}}$$
$$SR = \frac{\partial V}{\partial t} = \frac{1A}{20\,\mu F} = 50\,mV/\mu s \tag{3.1}$$

When the input of the ADC is directly connected to the output of DC-DC converters, the maximum voltage step at the ADC input per switching cycle is 50 mV. The voltage slew rate at the output of DC-DC converters is definitely limited by two parameters, which are the maximum current change and the output capacitance.

According to the analysis above, we can observe that the application of typical Nyquist ADCs is totally unnecessary. The Nyquist ADCs consume excessive power by performing the binary search over the full scale range, whereas the unit step swing at the output voltage of DC-DC converters from rail-to-rail supply voltages will never happen due to the limited SR. Hence, the Tracking ADC provides an optimal solution for digitally assisted DC-DC converters. In accordance to the output features of DC-DC converters, we propose our delta-encoded ADC that operates at a minimum clock frequency of 12.5 MHz. By defining the LSB of 5 mV the minimum slew rate of the digital output of the delta-encoded ADC is 62.5 mV/s, which is greater than the maximum voltage variation at the output of DC-DC converters.

Fig. 3.2 shows the architecture of a synchronous current-mode delta-encoded or Tracking ADC. The building blocks of the ADC are the main comparator, a current-mode DAC (I-DAC) and digital counter control logic. Based on a thermometer-coded current DAC, the input current converted by the input resistor is compared with the I-DAC current by the main voltage comparator (Comp). Upon the output of the main comparator the counter ramps up or down one LSB unit current of the I-DAC during one clock cycle to compensate the input current, until the equilibrium state is achieved so that the input current is equal to the I-DAC current. The unit current of the I-DAC is set to 250 nA and is scalable by setting the bias current from 100 nA to 400 nA. Through the input resistor of 20 kΩ the LSB unit voltage can be defined in the range from 2 mV to 8 mV to facilitate diverse applications.

This ADC has the single-ended input. Compared with the structure of fully differential inputs, the single-ended input suffers relatively from high noise, whereas dissipating half power. Furthermore, this ADC operates in current mode instead

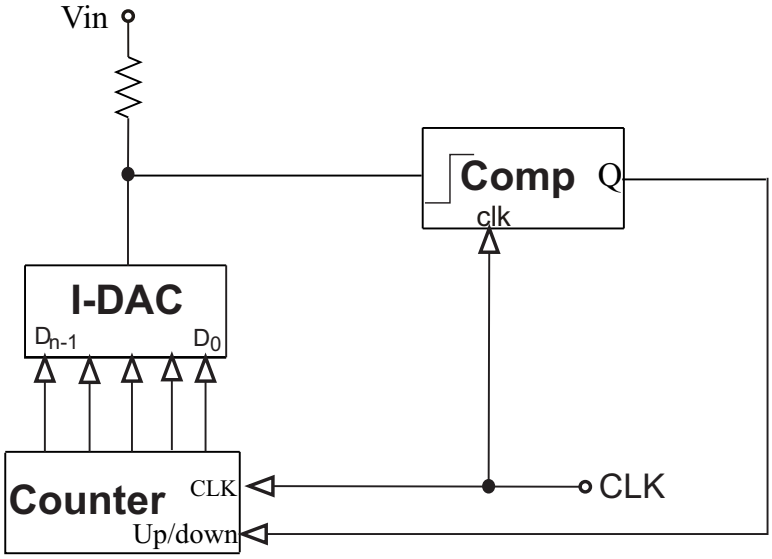

Figure 3.2: Current-mode Tracking ADC

of voltage mode, because current mode converters are an efficient solution for low power and high-speed (up to 100 MHz [45, 46]) ADCs. The main advantages of the efficiency rely on the facts, that, first of all, the current mode converter relaxes the requirements placed on the low supply voltage with the improperly scaled threshold voltage. In other words, the modern sub-micron technologies with the low supply but high threshold voltage constrains the desirable signal swing range. Secondly, by using current instead of voltage to represent the signal, the requirement for the resolution of comparators in the current mode can be more relaxed. Comparators in Nyquist ADCs determine the resolution of ADCs. In order to keep the same dynamic range in the ADCs with low supply voltage, the LSB unit voltage has to be scaled proportionally with the reduced signal operation range. However, the scaled LSB is very difficult to be identified by the comparators, because the input-referred thermal noise of MOS transistors is kept almost constant with scaling of MOS technology. So the input-referred thermal noise of comparator in the wideband frequency may overwhelm the low LSB voltage. But by the use of unit currents as operation signal such constrains can be easily overcome. The unit current in the range of nano ampere can be converted to a large voltage by a resistor, which we defines specifically. Meanwhile, the process operations of addition, subtraction and integration in the current mode are also easily implemented as in the voltage mode.

3.1.2 Self-clocked Tracking ADC

In addition to the limited output slew rate of DC-DC converters, another feature of DC-DC converters is, when they are in the steady-state, the output of DC-DC converters produces the expected DC voltage with the limited and small switching ripple. But once the disturbance as the load step occurs abruptly at the output of DC-DC converters, the output voltage varies significantly and fast. Hence, to avoid missing of important information and to provide significant data to the DSP promoting the digital feedback control to response simultaneously, the Tracking ADCs have to increase their data conversion rate.

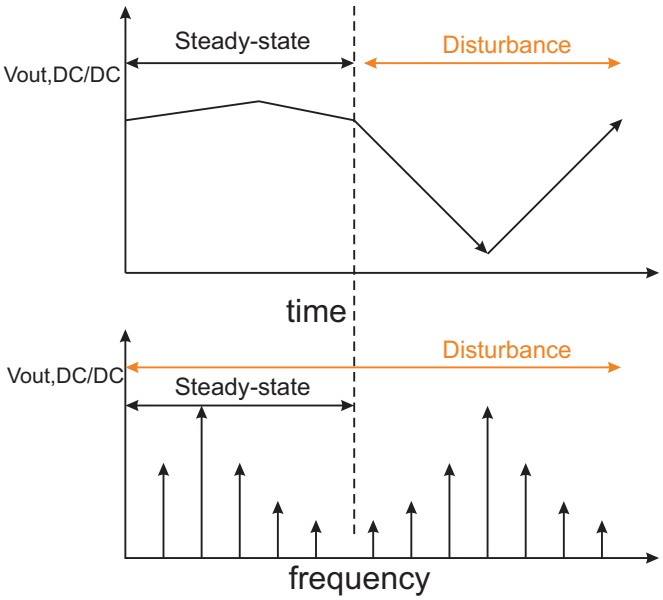

Figure 3.3: Frequency spectrum at the output of DC-DC converters in steady-state (left) and under disturbance (right)

But the synchronous Tracking ADCs used today are constrained by their general disadvantage that is the trade-off between high conversion rate and high power dissipation. As shown in Fig. 3.3, the output of DC-DC converters in the case of load step has wide bandwidth in the frequency domain, which is far away outside the output signal in the steady-state. In order to track the output of DC-DC converters concurrently, the sampling frequency of the synchronous Tracking ADCs has to cover at least twice the output bandwidth of DC-DC converters. As a result, the synchronous Tracking ADCs have to be clocked at their maximum frequency during the whole signal processing, whereas for the most time DC-DC converters work actually in the steady-state. The utilization of synchronous

Tracking ADCs in this case results directly in unnecessary power dissipation. To overcome the above mentioned limitations of synchronous Tracking ADC and to reduce the excessive power dissipation, a novel mechanism of transient-driven self-clocking ADC is presented in this work.

3.1.3 Transient-driven Tracking ADC

The delta-encoded ADC with transient-driven self-clocking is presented in Fig. 3.4. Based on the synchronous current-mode Tracking ADC shown in the Fig. 3.2, the new architecture of this ADC is derived by adding two auxiliary comparators and an asynchronous digital control logic to the synchronous current-mode Tracking ADC.

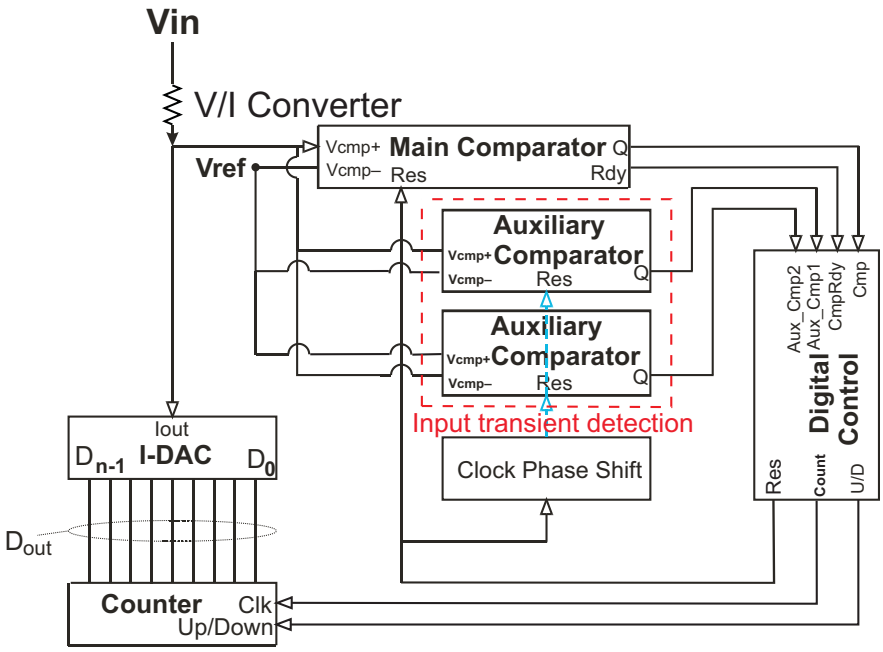

Figure 3.4: Block diagram of the asynchronous ADC

As already explained in section 3.1.2, a voltage-to-current converter (V/I) is implemented by one input resistor of 20 kΩ. The input current is compared with the I-DAC current. Depending on the output of the main comparator, one LSB unit current of the I-DAC will be ramped up or down by the digital control block, until the equilibrium state between the input current and I-DAC is achieved. Finally the input current should match the I-DAC current. As the synchronous current-mode ADC mentioned above, the unit current of the I-DAC in this case is also 250 nA and can be adjusted by external bias current from

100 nA to 400 nA. Additionally, all of comparators including main and auxiliary are dynamic latched comparators. When the clock input **Res** is rising from logic low up to logic high, the main comparator as well as auxiliary comparators are regenerated from the reset mode to perform the comparisons. Once the comparison of the main comparator is valid and settled at the rising edge of **Res**, a comparison result will be produced at the output **Q**. Moreover, the other output **Rdy** in the main comparator, which indicates the end of comparison cycle, will be also generated to be logic high. The power consumption of the whole ADC is mainly due to dynamic performance of latched main and auxiliary comparators, while the power dissipation from I-DAC, counter and asynchronous control circuit is quite minimized.

The clock of the ADC is asynchronously self-generated as shown in Fig. 3.5. In contrast to the synchronous ADC the asynchronous clock is variable during the signal processing. The clock period, as well as the latency, is adjustable in accordance to the event and conditions of applications. In other words, only an asynchronous clock can achieve both low feedback latency and low power dissipation beyond the Shannon-Nyquist requirements.

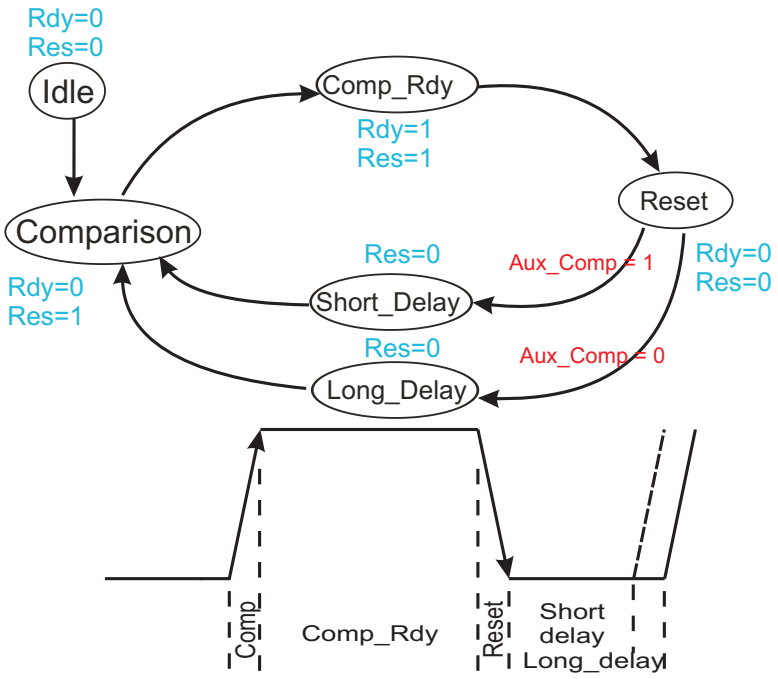

Figure 3.5: State machine of delta-encoded ADC

Initially the main comparator is triggered by the rising edge of **Res** from *Idle* state into *Comparison* state to start comparing the input signal. Once the

comparison of main comparator is settled and the output is valid, the settling detection of the main comparator sends a ready-signal **Rdy**=1 to the control logic input comparison-ready **CmpRdy**. Once entering the state of comparator-ready *Comp_Rdy* and waiting a very short settling delay time, the main comparator will be reset by the clock state machine. Meanwhile, the main comparator output **Rdy** as well as **Res** are also cleared to 0 or logic low. Afterwards, the signals of **Rdy** and **Res** are delayed by passing through the states *Short_Delay* or *Long_Delay*, which is selected by the outputs of the auxiliary comparator. If either output of both auxiliary comparators is logic high, the *short_delay* state will be selected. Otherwise, the *long_delay* state is chosen. Through one of the delay states the clock or **Res** signal is fed back to the *Comparison* state, where the main as well as auxiliary comparators are triggered again to start a new operation cycle.

The I-DAC is adjusted by the counter. The signals of **Clk** and **Up/Down** in counter are controlled by the outputs **Rdy** and **Q** of main comparator through digital control block respectively. Once the signal **Rdy** of main comparator is set to logic high, the **Clk** input of counter will be triggered. At the same time the **Up/Down** input of counter samples the value of **Q** of main comparator through digital control block, increasing or decreasing one unit current source incrementally.

The period of asynchronous clock is determined by the consecutive four states. However, *Comparison* and *Reset* states represent the rising and falling edges of clock among the four states. Their durations are only a fraction of nano seconds, which can be neglected. Hence, the period of asynchronous clock is mainly determined by the states of *Short_/Long_Delay* and *Comp_Rdy*.

The states of *short_/long_Delay* are implemented by the delay inverter rings, which will be explained in the successive sections. The selection of corresponding delays is determined by the mechanism of the input transient detection, which comprises two auxiliary comparators. The auxiliary comparator has an internally defined threshold voltage of 15 mV. Both Auxiliary comparators are cross-connected to create the threshold window of 30 mV to detect the input slope. The threshold window bounding the reference voltage of main comparator determines whether the tracking error of this ADC crosses the threshold windows seen in Fig. 3.6. If exceeded, which means that the input varies fast, one of the auxiliary comparators produces a logic high at the output. As a result, the *Short_Delay*

state will be selected to reduce the clock cycle. Otherwise, the I-DAC clock frequency will be kept as low as possible by choosing the *Long_Delay* state to minimize the energy consumption. Furthermore, to avoid disturbances caused by kickback noise between the main and the auxiliary comparators, the auxiliary comparators are operated on the inverted clock.

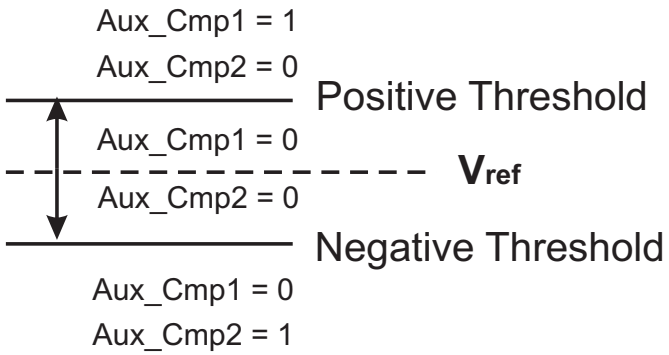

Figure 3.6: Operation range of the input signal transient detection

The state of comparison-ready *Comp_Rdy* presents the time of settling the comparison required by the comparators. If the ADC is operated by a synchronous clock applied externally, the clock period needs to be larger than the settling time of the comparator at least. For the fast mode application where the highest speed operation needs to be achieved, this issue would cause unnecessary timing restrictions. In particular, the settling time of a comparator is variable and dependent on the input signal. More precisely, the settling time of the comparator with larger differential input signal is essentially shorter than the comparator with smaller input signal, as shown in Fig. 3.7.

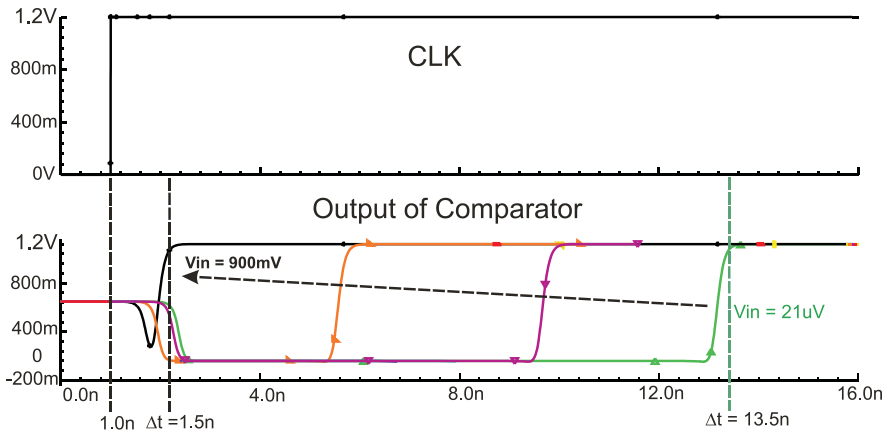

Figure 3.7: Settling time of comparators with different input voltage

By the use of an asynchronous concept in this work this issue of the settling time of the comparator can be solved. As seen in Fig. 3.5, once the comparison of main comparator is valid and settled, the generated clock signal is leaving directly logic high phase and waiting in logic low phase. So that the settling time of comparator represented by the state of *Comp_Rdy* achieves the minimum required value for correct operation of comparators.

Along with both delay states and comparator's settling time, the corresponding frequency of this ADC alternates between 12.5 MHz and 50 MHz, depending on the input transient variation. The slew rate of the digital output value in this ADC can be increased up to 250 mV/μs. Once a disturbance occurs at the output of DC-DC converters, it will be sensed by transient-driven ADC, which increases the conversion rate to improve the fidelity of tracking of the analog input signal. But if the output voltage of the DC-DC converter varies slowly, the clock frequency of the ADC is kept by this mechanism at a low sampling rate. This mechanism does not only improve the conversion characteristics of the ADC, but also the dynamic power efficiency, because the average sampling rate in the whole time domain is reduced considerably.

3.1.4 Input bandwidth

The input bandwidth of the transient-driven Tracking ADC is extended by the mechanism of threshold window. The Tracking ADC processes one LSB data conversion during one clock cycle. If the input of the Tracking ADC crosses more than one threshold level in less than one clock period, the traditional synchronous Tracking ADC can not follow the signal variation simultaneously. So the slope overload distortion will occur in the second sample [47].

To prevent the ADC from signal slope overload, the input signal slew rate is limited to

$$\left|\frac{\delta V_{in}}{\delta t}\right| < \frac{LSB}{1/f_{sample}} = \frac{V_{FS}/\left(2^B - 1\right)}{1/f_{sample}} \tag{3.2}$$

where V_{FS} is the full scale input range and B is the resolutions of the ADC, respectively.

Assuming that a sinusoidal signal is applied to the input, the maximum slope of the input should be at the zero crossing. If $f_{in,max}$ and V_{amp} present the maximum bandlimited frequency of the input and the maximum amplitude of the

input respectively, Eq. 3.2 can be solved as:

$$\left|\frac{\delta V_{in}}{\delta t}\right| = \left|\frac{\delta\left(V_{amp}\sin\left(2\pi f_{in,max}t\right)\right)}{\delta t}\right|_{t\cong 0} = V_{amp}\cdot 2\pi f_{in,max} \tag{3.3}$$

Defining that V_{amp} is equal to $V_{FS}/2$ and applying Eq. 3.2 to Eq. 3.3, we get

$$f_{in,max} = \frac{f_{sample}}{2^B\cdot\pi} \tag{3.4}$$

For a given resolution of the ADC, the maximum input frequency is proportional to the sampling frequency of the ADC. In the case of DC-DC converters, where the output of DC-DC converters varies significantly due to occasional load steps, for instance, but remains stable during the rest of the time, the sampling frequency of nominal synchronous Tracking ADCs must be set considerably higher to cover the high input frequency, which corresponds to high power dissipation.

In transient-driven Tracking ADCs, this constrain is improved, because the sampling frequency varies during the data processing. As mentioned above, if the input signal varies very fast and exceeds the threshold window, the sampling frequency of this ADC is switched from 12.5 MHz of the *nominal mode* to 50 MHz in the *fast mode*. Otherwise, the sampling frequency of this ADC remains unchanged in its *nominal mode*, as long as the tracking error between the input voltage and DAC feedback is within the range of the threshold window.

With a LSB of 5 mV the maximal input frequency varies from 62 kHz to 249 kHz. Meanwhile the slew rate of the output of the transient-driven Tracking ADC is increased from 62.5 mV/μs up to 250 mV/μs.

3.2 Stability

Whenever a feedback loop appears in circuits, the issue of stability must be considered. This is also applicable to our proposed ADC with two feedback loops, which are particularly critical to the stability. This section discusses stability issue of the proposed ADC.

3.2.1 Modeling of the proposed ADC

The presented delta-encoded ADC comprises two feedback loops to realize the transient-driven self-clocking performance. As mentioned in Fig. 3.4, the interior loop triggers the comparison of the main and the auxiliary comparators, while

the outer loop tunes the output I-DAC incrementally to match the input current. Therefore, the counter in Fig. 3.4 is considered as discrete-time(DT)-integrator in this case. Depending on the outputs of both auxiliary comparators the delay path for fast and slow modes will be selected to determine self-clocked frequency. The main and auxiliary comparators can be considered together and modeled to one block for easy analysis, because they share the common self-clocked trigger to perform the comparison. So the function of main and auxiliary comparators is simplified as seen in Fig. 3.8, where τ_1 indicates the necessary delay path for self-clocking of this ADC.

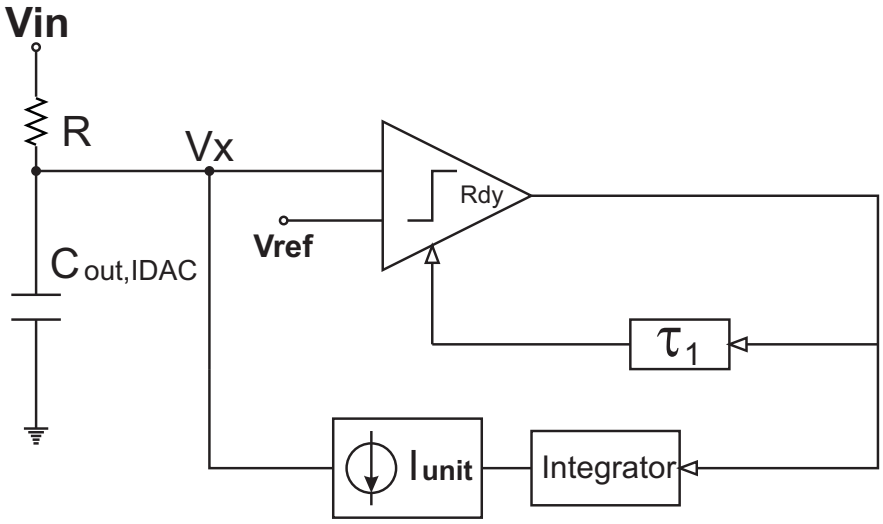

Figure 3.8: Modeling of the presented ADC with double feedback

Generally multi-feedback loops appear mainly in multi-input multi-output system (MIMO) instead of single input and output system. But if we consider the details of this ADC again in Fig. 3.4, it is found that the counter or DT-integrator is synchronized with the main comparator. Related to the clock of the main comparator, the clock trigger to the counter or DT-integrator is delayed by the settling time required by the main comparator. Given this fact, the two feedback loops in terms of self-clocking can be modeled as single loop feedback shown in Fig. 3.9.

So far, the presented ADC is modeled similarly to synchronous ADCs. However, this ADC is self-clocked and asynchronous, and the self-clocked frequency is not constant during the signal processing. To avoid confusion, we focus on the fast mode, in which the ADC is self-clocked at its highest available frequency

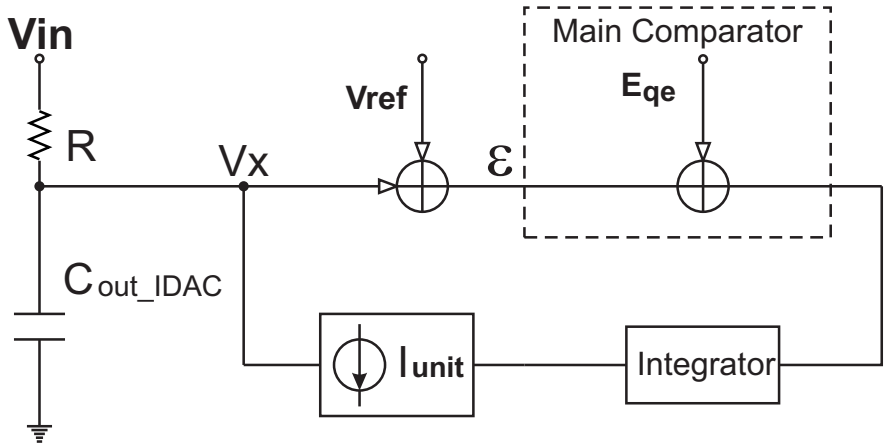

Figure 3.9: Remodeling of proposed ADC with one closed feedback loop

of 50 MHz. Because if the ADC works stable in the fast mode for high speed operation, it can also work stable in the slow mode at the low clock frequency.

To answer the question of stability for this ADC, we must consider whether the voltage of V_x can be settled during one clock period of comparators, so that the error signal ε is always kept below a half LSB. The verification of stability could be performed by means of miscellaneous criteria in terms of frequency response. Among them "Barkhausen's Criterion" is one suitable option, especially for single loop feedback as shown in Fig. 3.10.

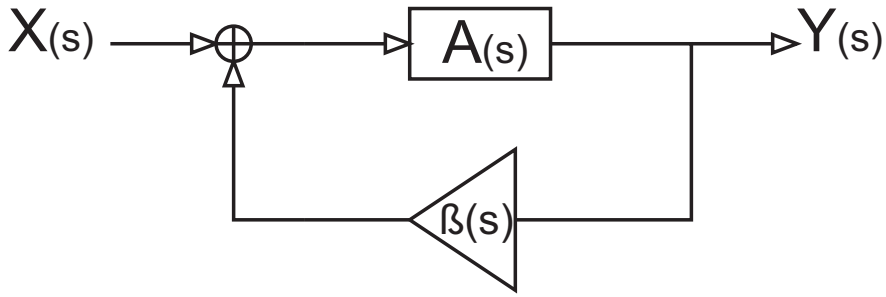

Figure 3.10: Basic negative feedback system

The basic principle of this criterion means that the gain goes to infinity and the circuit begins to oscillate, when

$$\left|\beta_{(s)} \cdot A_{(s)} = 1\right| \tag{3.5}$$

$$\angle\beta_{(s)} \cdot A_{(s)} = -180^\circ \tag{3.6}$$

To prevent an undesired oscillation, the loop gain must have a magnitude less than one at a phase shift of 180°, or the phase shift must be smaller than 180°,

when the gain is one. Only if this requirement is fulfilled, the system can work stable and achieve the expected performance.

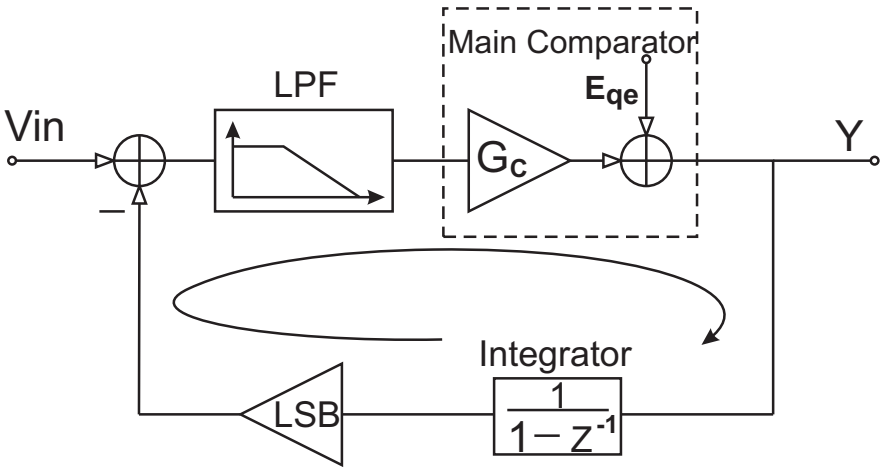

Figure 3.11: Small signal modeling of proposed ADC with open loop feedback

According to the model of Fig. 3.9, the signal flow is derived in Fig. 3.11, where the voltage of the output is fed back. The LSB represents an LSB voltage of $I_{unit} \cdot R$. The non-delaying integrator is operated at the same frequency of 50 MHz as the main comparator. When the output of main comparator is integrated by the counter, the feedback voltage is subtracted from the input V_{in}. At the input node of the comparator the resistor of the V/I-converter and the output capacitance of the I-DAC create a RC-lowpass filter ("LPF" in Fig. 3.11). The RC-lowpass filter (see Fig. 3.9) delays the settling of the LSB voltage unit step before it is passed to the input of the main comparator. Then a linearized comparator with average gain (G_C) and quantization error (E_{qe}) amplifies the voltage error and converts it to digital logic level.

The low pass filter (LPF) can be described as:

$$f_{lp(s)} = \frac{\frac{1}{s \cdot C_{out\_IDAC}}}{R + \frac{1}{s \cdot C_{out\_IDAC}}} = \frac{1}{1 + \frac{s}{s_{-3dB}}} \tag{3.7}$$

where

$$s_{-3dB} = \frac{1}{R \cdot C_{out\_IDAC}}$$

Meanwhile, in the steady-state of ADC the output of the LPF is equal to or less than a half LSB unit. So the average gain for linearized comparator is:

$$G_c = \frac{V_{dd}}{V_{LSB}} \tag{3.8}$$

where $V_{dd} = 1.5\,V$ in this work, and $V_{LSB} = I_{unit} \cdot R$. So the open loop transfer function could be presented as:

$$H_{(s)} = f_{lp(s)} \cdot G_c \cdot \frac{1}{1 - z^{-1}} \cdot V_{LSB} \tag{3.9}$$

Inserting Eq. 3.16 and Eq. 3.8 in Eq. 3.9, the open loop transfer function is written as:

$$\begin{aligned} H_{(s)} &= \frac{1}{1 + \frac{s}{s_{-3dB}}} \cdot \frac{V_{dd}}{V_{LSB}} \cdot \frac{1}{1 - z^{-1}} \cdot V_{LSB} \\ &= \frac{V_{dd}}{1 + \frac{s}{s_{-3dB}}} \cdot \frac{1}{1 - z^{-1}} \end{aligned} \tag{3.10}$$

3.2.2 Frequency response

The frequency response is determined mainly by the low pass filter and the integrator. The integrator is a non-delaying integrator, which means that there is no delay between input and output of the integrator. The counter or integrator operates in discrete-time domain and is expressed in z-domain. But to explore the characteristics of the magnitude and phase responses we must express the frequency characteristics of the integrator:

$$H_{integrator} = \frac{z}{z - 1} \Rightarrow \frac{e^{j2\pi \frac{f}{f_s}}}{e^{2\pi \frac{f}{f_s}} - 1} \tag{3.11}$$

With Eulers formel the transfer function of a non-delaying integrator is expressed as:

$$H_{integrator} = \frac{\cos\left(2\pi \frac{f}{f_s}\right) + j \sin\left(2\pi \frac{f}{f_s}\right)}{\left(-1 + \cos 2\pi \frac{f}{f_s}\right) + j \sin\left(2\pi \frac{f}{f_s}\right)} \tag{3.12}$$

The magnitude of integrator is

$$\begin{aligned} |H_{integrator}| &= \frac{1}{\left|\left(-1 + \cos 2\pi \frac{f}{f_s}\right) + j \sin\left(2\pi \frac{f}{f_s}\right)\right|} \\ &= \frac{1}{2\left|\sin \pi \frac{f}{f_s}\right|} \end{aligned} \tag{3.13}$$

The phase of integrator can be written:

$$\angle H_{integrator}(f) = \angle(nom) - \angle(denom)$$

After using trigonometric relations ($\cos(2x) = 1 - 2 \cdot \sin(x)^2$, $\sin(2x) = 2 \cdot \sin(x)\cos(x)$), the phase response of integrator is derived as:

$$\angle H_{integrator}(f) = 2\pi\frac{f}{f_s} - \left(\frac{\pi}{2} + \pi\frac{f}{f_s}\right) = \pi\frac{f}{f_s} - \frac{\pi}{2},\ 0 < f < f_s \tag{3.14}$$

According to the Eq. 3.13 and Eq. 3.14, the frequency response of integrator sampling at 50 MS/S is shown in Fig. 3.12.

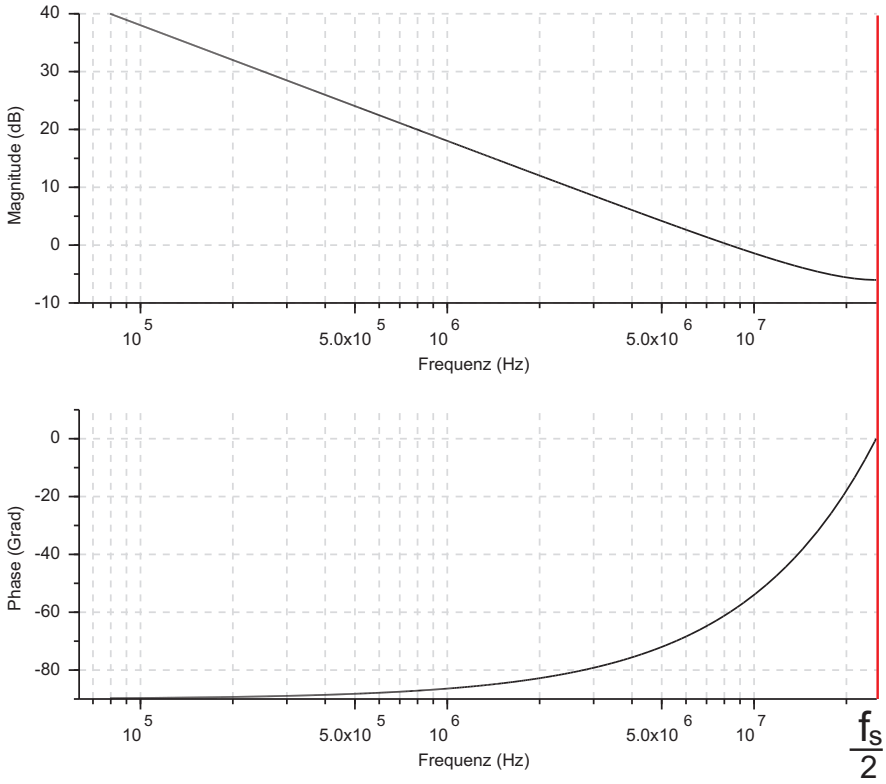

Figure 3.12: Frequency response of non-delaying integrator

At the DC state the phase contribution of integrator is $-90°$, while at the Nyquist frequency, which is default defined in discrete-time domain as $f_s/2$, the phase shift is 0°. To achieve the sensible stability of the ADC, the phase margin of the open loop at the frequency, where the magnitude is equal to one, should be about 70°. At -3 dB frequency the low pass filter contributes $-45°$

$$\angle LPF(f_{-3dB}) = -45° \tag{3.15}$$

If the phase margin of the open loop should be 70°, the allowed phase of the integrator can be calculated:

$$70° = 180° + \angle LPF(f_{-3dB}) + \angle LPF(Integrator)$$
$$-110° = -45° + \angle LPF(Integrator)$$

then

$$\Rightarrow \angle(Integrator) = -75^\circ \tag{3.16}$$

Referred to Fig. 3.12, we can approximately obtain that the pole frequency of low pass filter should coincide with the frequency of integrator, which is equal to or larger than 5 MHz.

From Eq. 3.15 the -3 dB frequency of the first-order low pass filter in this work is derived as:

$$f_{-3dB} = \frac{1}{2\pi\,(R \cdot C_{out\_IDAC})}$$

Applying $f_{-3dB} = 5$ MHz and $R = 20\,k\Omega$ to the equation above, we get

$$C_{out\_IDAC} \leq \frac{1}{2\pi\,(R \cdot f_{-3\,dB})} \cong 1.55\,pF \tag{3.17}$$

After analyzing the frequency response of integrator and estimating the maximum allowed capacitance, all of the sub-blocks could be combined together to verify the characteristics of the open loop. However, Eq. 3.10 comprises continuous and discrete-time domains, which are not compatible for the verification simultaneously. Thus, one of them must be transformed into the other domain. Applying the Fig. 3.11 to Fig. 3.10, where f_s represents the sampling frequency of 50 MHz, the open loop transfer function in the s-domain is illustrated in Fig. 3.13

Despite that the phase margin at the unit magnitude is 60°, which is about 10° smaller than we calculated in Eq. 3.16, the stability of our ADC is not disturbed by the small deviation. Additionally the capacitance used in the Fig. 3.13 is set to the maximum allowed value. But the practical parasitic capacitance from the design is smaller than 1.55 pF as mentioned in Eq. 3.17. So using the extracted value of parasitic capacitance of 0.27 pF described in the script below, the actuall -3 dB frequency of the LPS is about 28 MHz. Therefore, the phase margin is increased up to 100° as seen in Fig. 3.14.

By all means, from Fig. 3.13 and Fig. 3.14 we can ensure that as long as the parasitic capacitance is smaller than the maximum value of 1.55 pF, our ADC is always kept stable.

The script describing the frequency response of open loop of the proposed ADC is listed below. The simulation system tool is recommended to use ScicosLab 4.4.1.

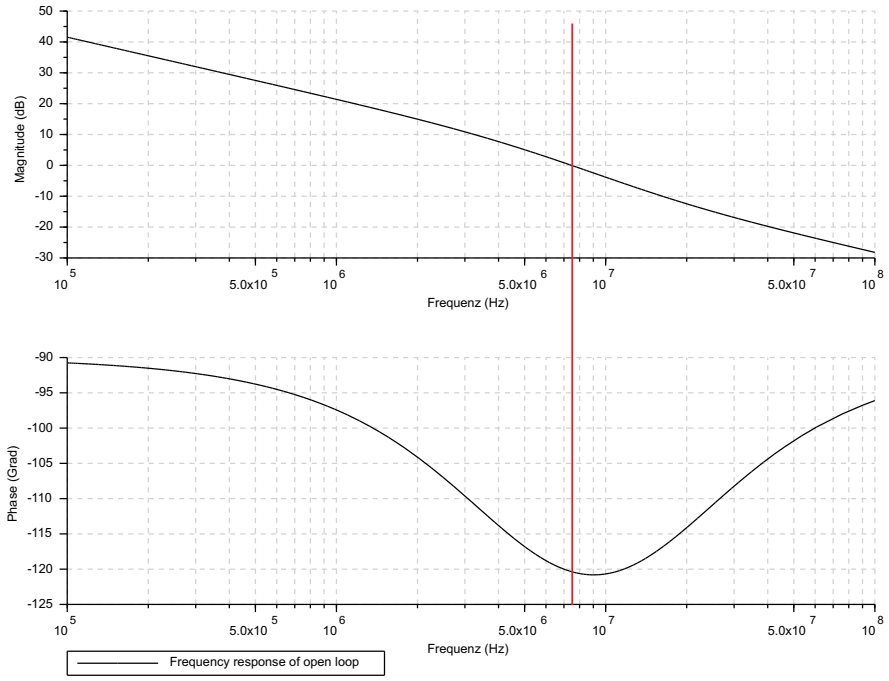

Figure 3.13: Open loop frequency response of the presented ADC with maximum allowed capacitance

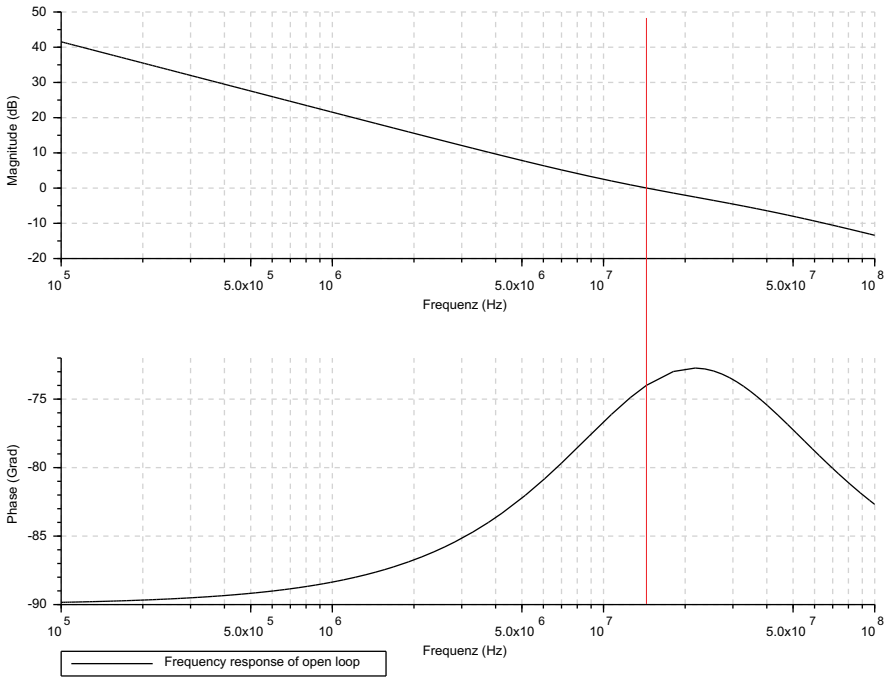

Figure 3.14: Open loop frequency response of the presented ADC with capacitance extracted from design

```
//------beginning ----------------------
z       = poly(0,'z');
s       = poly(0,'s');}
//------LSB ----------------------------
// the LSB unit current source is 250 nA
Iun     = 250e-9;
// the input resistance is 20 kOhm
R       = 20e3;
// the lsb unit voltage is 5 mV
Vlsb    = Iun*R
//------Low pass filter ----------------
// the capacitances are caused by cascode,
// mirror transistor and input of comparator.
//1. capacitance of mirror transistor
cdd_m   = 1.012e-15;
cgd     = 1e-15;
c_m     = cdd_m + cgd;
//2. capacitance of cascode transistor
cdd_cas = 0.37e-15;
cgd     = 0.33e-15;
c_cas   = cdd_cas + cgd;
//1+2. capacitance of unit current source
Cunit   = c_m + c_cas
//3. capacitance of input transistor of comparator
cdg     = 5e-15;
cgg     = 17.6e-15;
cgs     = 9e-15;
Ccom    = cdg + cgg + cgs
//------the total capacitance-----------
Ctotal  = 65*Cunit + 3*Ccom
//Ctotal  = 1.55e-12;
//plot the continuous-time system in transfer form
S_3db   = 1/(R*Ctotal);
f_3db   = S_3db/2/%pi;
f_lp1   = 1/(1+s/S_3db);
f_lp1   = syslin('c', f_lp1);
scf(1);
clf(1);
bode(f_lp1,1e4,1e9,'flp1');
//------averaged gain of comparator-----
Orms    = 1.5;
Verr    = Vlsb;
Gc      = Orms/Verr;
f_comp  = Gc;
//---non-delay integrator in the feedback loop---
Tsample   = 20e-9;
//------d2c transformation---------------
f_ing_t = z/(z - 1);
f_ing_t = syslin(Tsample, f_ing_t);
f_ing_t = horner(f_ing_t, (2+s*Tsample)/(2-s*Tsample));
//------open loop transfer function-----
H       = f_lp1*f_comp*f_ing_t*Vlsb;
```

```
H       = syslin('c', H);
scf(2);
clf(2);
bode(H, 1e5, 1e8,'Frequency response of open loop');
```

3.3 Dynamic behavior

Before we begin with concrete circuit design, the new concept must be verified. The characteristics must comply with the frequency response and the transient behavior requirements. Nowadays different approaches can be used to accomplish this task, for instance, Verilog-A and Simulink (Matlab). But no matter what kind of software, all of them apply the mathematical algorithm to describe the ideal functional behavior of circuits, verfying its dynamic behavior over time. In this work ScicosLab 4.4.1 is used to perform this verification, and this system tool is freeware.

3.3.1 Dynamic system

The specific introduction of a dynamic functional modeling of the proposed ADC is described in Fig. 3.15. This system model consists mainly of four blocks, which are digital control, main and auxiliary comparators, as well as V/I converter and IDAC. The integrator, IDAC and V/I Converter, which are already shown in Fig. 3.4, are combined together in one functional block $V/I\,converter\,\&\,IDAC$. Its output depicted as V_{cmp+} will be compared by the main comparator as well as auxiliary comparators with the reference voltage to adjust the output of this ADC and the self-clocked frequency. The outputs of digital control block used as clock triggers to main comparator, auxiliary comparators and the integrator are depicted as **Res**, **Res_aux** and **CLK_IDAC** respectively. And these signals are featured as event impulse in this model, because the event signal as available activation signal in ScicosLab is used to activate the fundamental blocks to sample the input and to perform the signal processing.

The V/I Converter is implemented by one single resistor in the physical level and this resistor is connected with the output of IDAC. Due to the parasitic capacitance from IDAC and the associated comparators, the V/I Converter with the parasitic capacitance forms a low pass filter. To verify the frequency response, the maximum capacitance, which is extracted from the schematic of the proposed

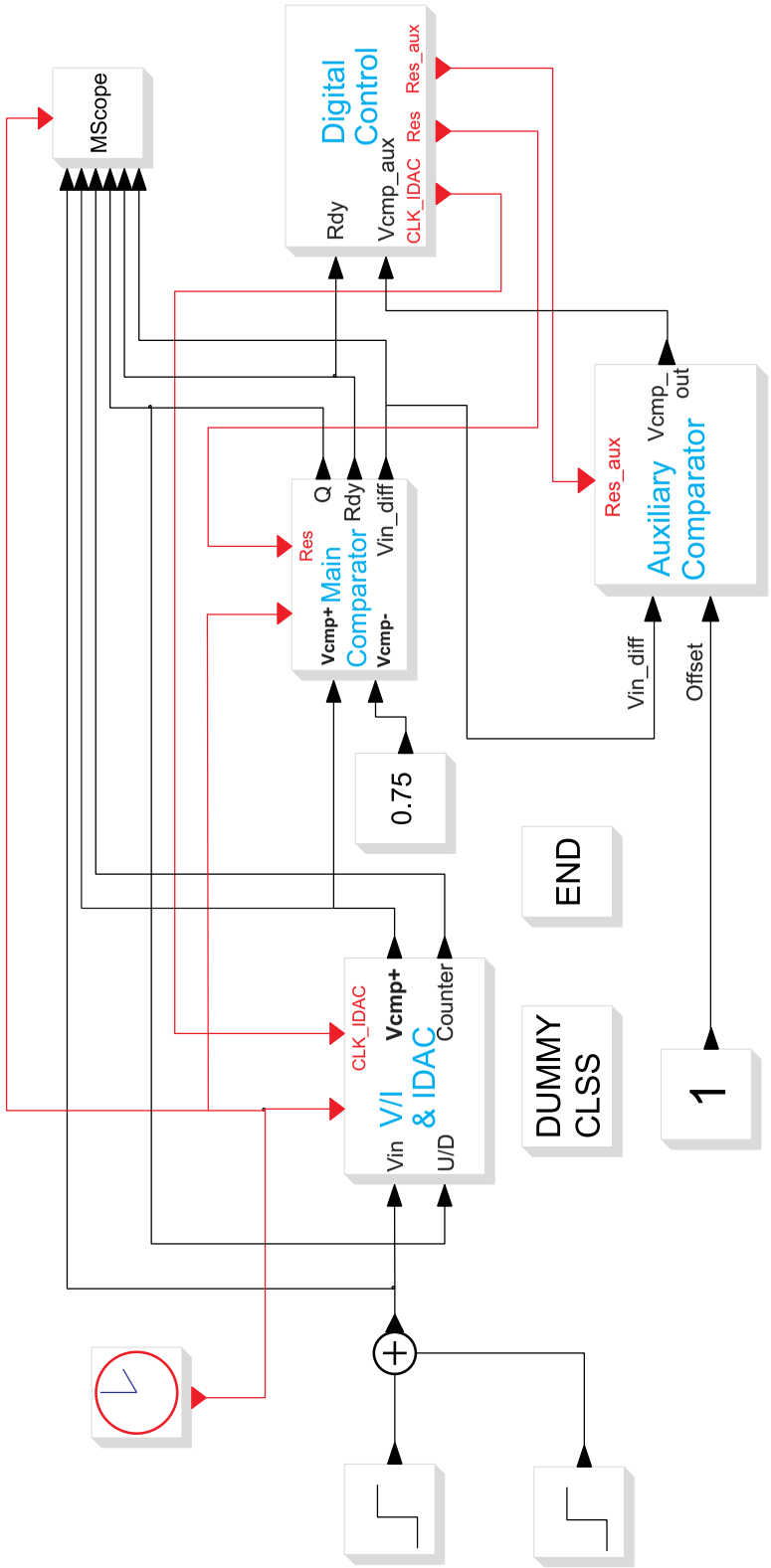

Figure 3.15: topology

ADC, is used in calculations of section 3.2.2. But for the exploration of the dynamic behavior, the currents of the IDAC and the associated parasitic capacitance will be switched on or off incrementally over time as the integrator output increases or decreases. Therefore, the working principle of $V/I\ converter\ \&\ IDAC$ can be also described as low pass filter shown in Fig. 3.16, but the number of unit current source and the associated parasitic capacitance in the integrator vary incrementally over time.

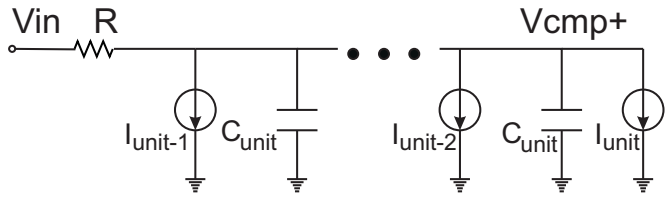

Figure 3.16: Low pass filter with variable current source

Depending on the output of the integrator, we get

$$\frac{V_{in} - V_{cmp+}}{R} = (V_{cmp+} \cdot sC_{unit} + I_{unit\_1}) \cdots (V_{cmp+} \cdot sC_{unit} + I_{unit\_2}) + I_{unit} \quad (3.18)$$

After rewriting the Eq.3.18, $V/I\ converter\ \&\ IDAC$ can be indicated as:

$$\begin{aligned} V_{cmp+} &= \frac{V_{in} - I_{unit} \cdot R - R \cdot (I_{unit\_1} + I_{unit\_2} + \cdots)}{1 + sR \cdot (C_{unit\_1} + C_{unit\_2} + \cdots)} \\ &= \frac{V_{in} - I_{unit} \cdot R - I_{unit} \cdot R \cdot G_{int}}{1 + sRC_{unit} \cdot G_{int}} \end{aligned} \quad (3.19)$$

Where G_{int} represents the integrator or counter, which incrementally switches on or off the unit current source in the IDAC.

In ScicosLab Eq. 3.19 can be realized in Fig. 3.17 by using fundamental mathematic operators. Besides, Eq. 3.19 considers mainly the effects of parasitic capacitances of IDAC. If the other parasitic effects need also to be taken into account, such as the input capacitance from comparators, this equation can be further used by modifying the denominator. Although Eq. 3.19 contains continuous variable as well as the integrator G_{int} in discrete-time domain, which is decribed as $1/(1 - z^{-1})$ in ScicosLab, both are still compatible and could be simulated simultaneously, because the ScicosLab is activated by the event impulse spread in time space.

The Main comparator is modeled in Fig.3.18. The behavior is described by the block of Scifunc, which is activated by event impulse driven pin of **Res** as

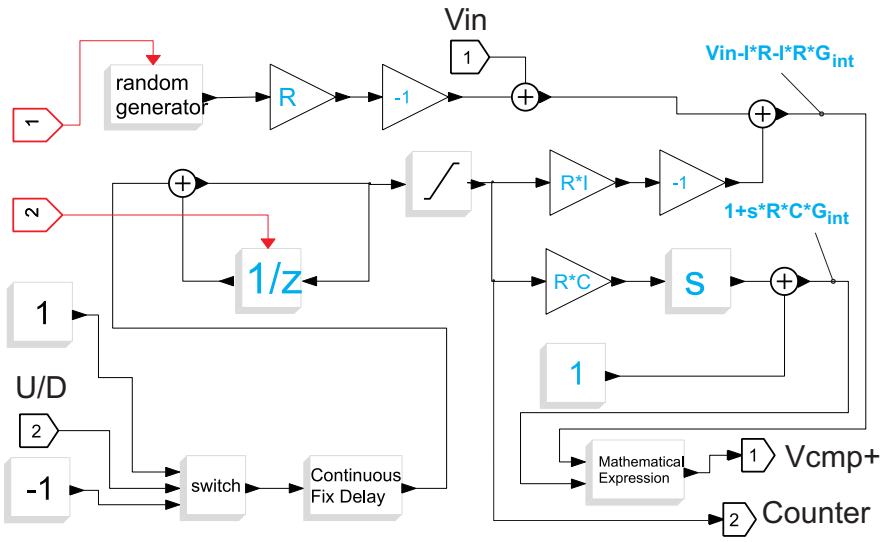

Figure 3.17: VIC and IDAC

clock trigger. If the differential input of the comparator Vin_diff is bigger than zero, output Q is logic high, otherwise logic low. Similar to the modeling of main comparator, the same architecture can be also applied to describe the behavior of auxiliary comparators. The auxiliary comparators have the input offset voltage to

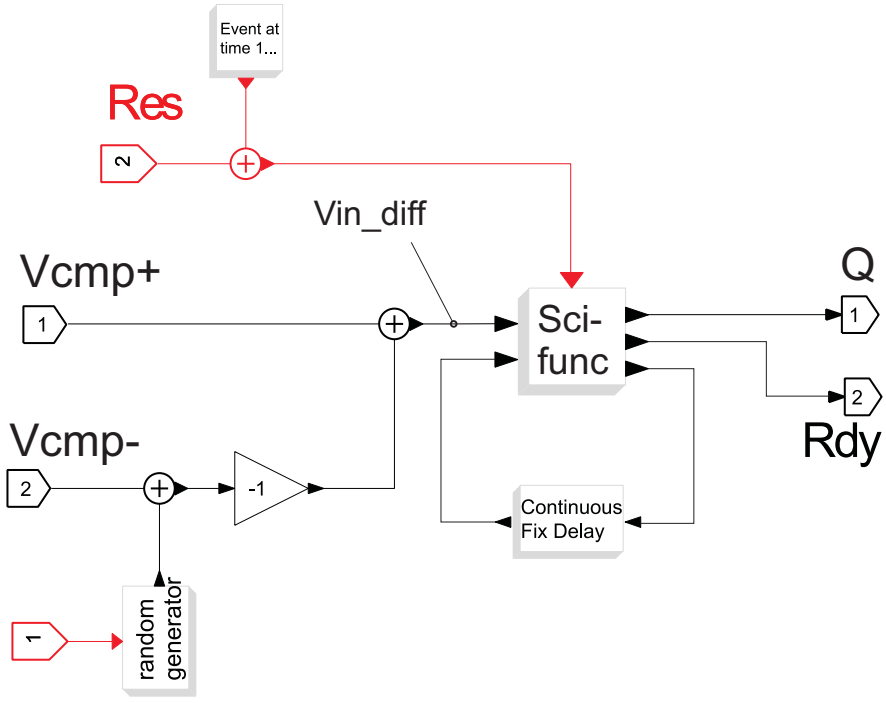

Figure 3.18: Functional model of main comparator

create the threshold window. For the functional model this operation is expressed by mathematical algorithms from the library of ScicosLab.

The digital control block shown in Fig. 3.19 produces the clock triggers for IDAC, auxiliary comparator and main comparator respectively. The clock triggers of ScicosLab are featured as event impulses. The clock triggers for comparators will be deferred either through fast mode or slow mode, depending on the outputs of auxiliary comparators. The blocks in dark shade are defined to be slow mode.

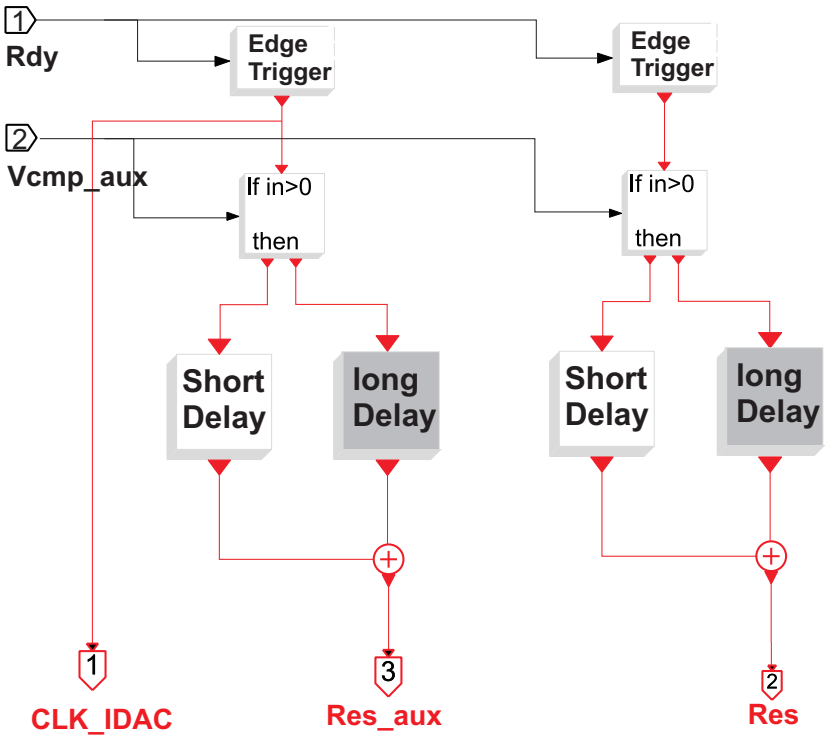

Figure 3.19: Functional model of digital control

3.3.2 Simulation of model

Fig. 3.20 shows the signals already defined in Fig. 3.4. It is seen that the negative input of main comparator V_{cmp-} is constantly set to 750 mV, while the input signal V_{in} is set to be 0.9 V initially, So the tracking error signal depicted as V_{cmp+} in this case, deviates significantly from its negative reference voltage V_{cmp-}. Due to the deviation that is larger than the threshold window of 30 mV defined by the auxiliary comparators, the clock frequency of the ADC is increased up to 50 MHz as expected. With the tracking error voltage reaching V_{cmp-} and returning into

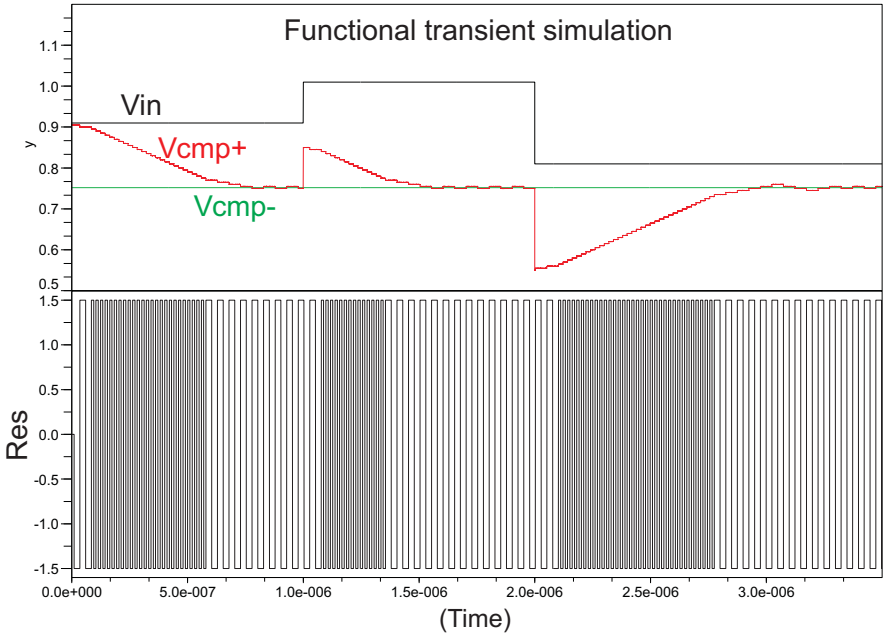

Figure 3.20: Transient verfication of functional behavior

the range of threshold window, the clock frequency is reduced again down to 12.5 MHz. At the time 1.0 μs V_{in} steps about 0.1 V up to 1.0 V and at the time 2.0 μs V_{in} steps again about 0.2 V down to 0.8 V. The clock signal behaves as

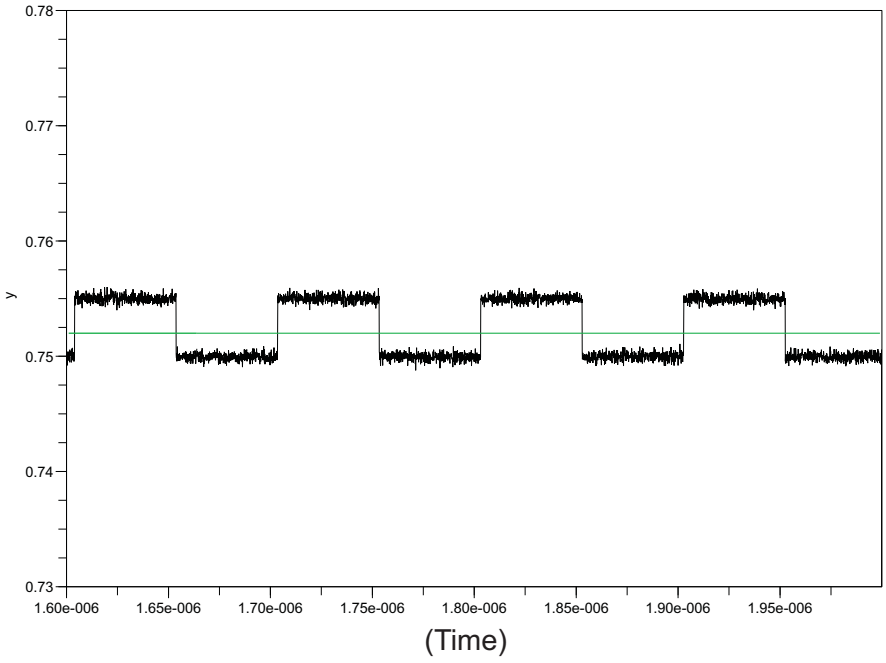

Figure 3.21: Stability of tracking error signal

same as in the beginning phase. In other words, as V_{in} varies fast, leading the tracking error signal to exceed the threshold window, the clock frequency is self-increased by the ADC. Otherwise, the ADC is operated in its nominal mode of 12.5 MHz, where the tracking error signal seen in Fig. 3.21 steps up and down one LSB around the reference voltage. Therefore, we can say that the new concept of the proposed ADC is proven to be realizable, and its dynamic signal flow matches also the specification as expected.

Chapter 4

Design of novel dynamic latched comparator

A comparator is widely used in different applications. Especially for ADCs the characteristics of comparators determine directly the resolution or dynamic range of ADCs. The mostly used comparators are latched comparator instead of continuous. The advantages of latched comparators are based on the positive feedback in the latch circuits, resulting in fast settling of comparison.

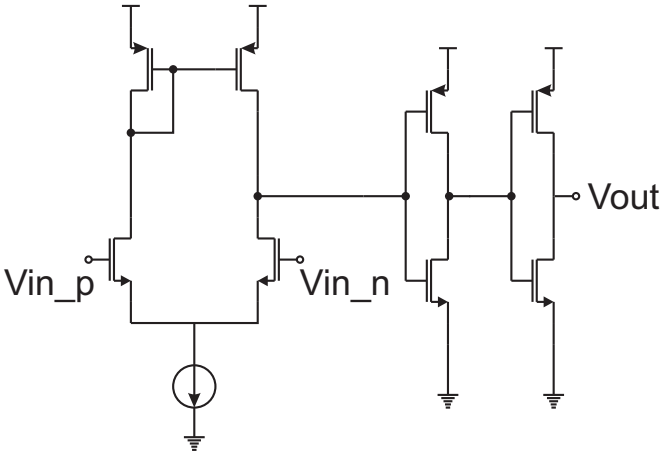

Figure 4.1: Continuous comparator

For continuous comparators shown in Fig. 4.1 the operational amplifier normally would be used to drive the successive inverter and generate the output. If continuous comparators are applied in high speed applications, an operational amplifier with high bandwidth is required, consuming a lot of power. This does not match our criteria of high power efficiency. Hence we restrict our search on latched comparators.

4.1 Kickback noise

Although the latched comparators perform faster than their continuous counter parts, they are predominantly limited by kickback noise, thermal noise and mismatching. These phenomena disturb the performance of latched comparators, limiting the dynamic range of ADCs.

Among the disturbances, kickback noise is a special problem, because it is related to the pre-amplifier and the input source. The root cause of kickback noise is due to the linking parasitic capacitance of MOS transistor. As seen in Fig. 4.2, the comparator is based on a regenerative latch of two inverters. In the reset phase, both inverters are shorted by the switch. Once the switch is opened, the positive feedback regenerates the outputs to supply rail voltages, respectively. But the large variation of output voltages produces large current spike that is fed through the gate-drain capacitance of the input transistors back to the input nodes. Across the input impedance the injected current produces a kickback noise voltage, which disturbs the input signal, as depicted in the Eq. 4.1. This kickback noise is called differential kickback noise.

$$\begin{aligned} I_{kickback} &= C_{gd} \cdot \frac{\Delta V_{var}}{\Delta t} \\ V_{kickback} &= I_{kickback} \cdot R_{input} \end{aligned} \tag{4.1}$$

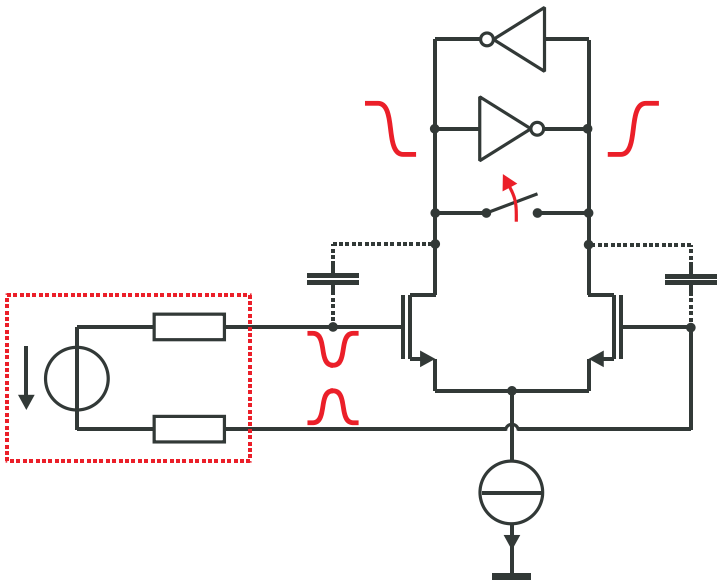

Figure 4.2: Root causes of kickback noise generation

In addition to the differential kickback noise, the clocked input generates also the common-mode kickback noise through the coupled capacitor, which comprises not only the gate-drain capacitance but also the gate-source capacitance. Especially when the input of comparators has an asymmetric impedance, the common-mode kickback has even worse effect.

In ADCs [48, 49], where the input impedances are asymmetric and comparators are connected in parallel, the common-mode kickback noise current over the asymmetric impedance considerably disturbs the input signal, leading to wrong decision results of comparators and limiting the performance of ADCs. Therefore, a novel dynamic latched comparator using common-source input transistors and a decoupling mechanism for reducing the common mode as well as differential kickback noise is presented in the following sections.

4.1.1 Analysis of latched comparator architectures

Before we go into the details of our comparator design, a review of available latched comparators will be useful to achieve an overview and background of comparators in terms of power consumption, speed and kickback noise. Commonly three kinds of latched comparators are used in the applications of ADCs, which are static, class-AB and dynamic latched comparators. Each of them has its own advantages or disadvantages compared to the others. Depending on the given requirement, the suitable comparator among them needs to be chosen specifically.

Fig. 4.3 shows the static latched comparator, which consists of a pre-amplifier and a latch stage. Similar to continuous comparator above, the advantage of this latched comparator is its low kickback noise, because the inputs are indirectly connected to the outputs by the preamplifier. But the speed of regeneration is limited by the current sources, and the preamplifier limits also the bandwidth of comparator and dissipates static current. To achieve the high bandwidth of the preamplifier for high-speed application, large static biasing current is necessary as in [50]. Therefore, the static latched comparator is nearly as consuming as continuous comparators in terms of power dissipation.

Compared to static latched comparators, the class-AB latched comparator shown in Fig. 4.4 settles much faster, because it has no pole caused by a preamplifier as in the static latched comparator. Furthermore, the cross-coupled inverters provide large current for the regeneration. A disadvantage is that the

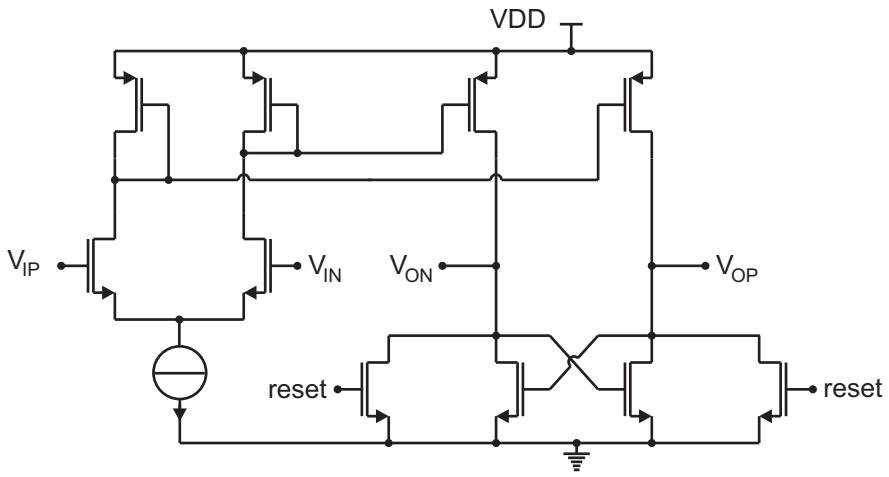

Figure 4.3: Static latched comparator

input transistors are directly connected to the output nodes that swing from rail-to-rail supply voltages respectively. So a high kickback noise is generated and injected through gate coupled capacitance to the input. In recent publications [51, 52] some improvements have been done. The basic principle is to decouple the input transistor from the outputs by active switches, before the differential output swings to its full level. But the required cascode transistors in [51] limit the common mode range and the Reduction Techniques II in [52] requires also an additional precise non-overlapping clock with accurate timing. Furthermore, the input stage dissipates always static power, which is unfavorable for our requirement regarding power efficiency.

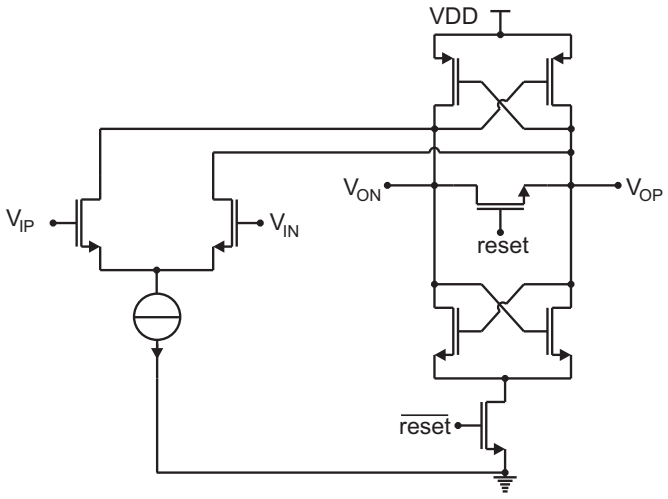

Figure 4.4: Class AB comparator

The typical dynamic latched comparator shown in Fig. 4.5 [49] is the most power-efficient comparator, because it has no pole at the preamplifier stage and no static current as the other latched comparators. This comparator performs also very fast due to the cross-coupled inverters, which provide large current as in the class-AB comparator. But it produces the highest kickback noise at the input. Not only the differential kickback noise as in the class-AB latched comparator, but also the common-mode kickback noise is very critical. This is caused by the large voltage variation of the Drain and Source (D/S) nodes of the input differential pair. In the reset phase, the drain nodes of the input pair (V_{Drain_P}/V_{Drain_N}) are reset to VDD and the source nodes of input pair (V_{Source}) float also at high voltage level; once the comparator is triggered into regeneration phase, the D/S nodes of input pair start falling. This large variation of falling D/S nodes of input pair produce large common-mode kickback noise through the gate capacitances of the input transistors. Furthermore, this comparator has four transistors in stack instead of three, slowing its settling speed and increasing its minimum supply voltage, when compared to the class-AB latched comparator.

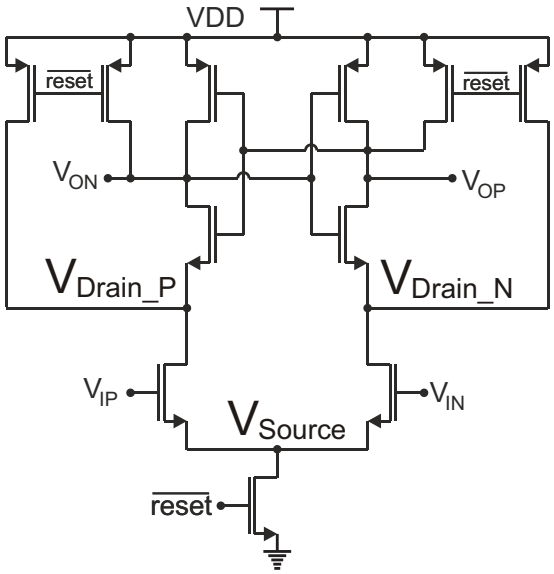

Figure 4.5: Dynamic comparator

The characteristics of differential kickback noise have been optimized by a double tail latched comparator [53], which is shown in Fig. 4.6. This comparator has two stage configuration. The first stage is dynamic clocked differential stage (bottom), and the second stage is a regeneration latch with common-source input

pair (M10/M11). In reset mode, where Clk is logic low, the voltages of Di+/− are pulled up to VDD. When Clk is rising from logic low to logic high, Di+/− start falling from VDD, and the first stage amplifies the slew rate difference. After regeneration Di+/− are pushed to ground, turning M10 and M11 off. So no static current will flow through the comparator. Compared to the traditional dynamic comparator, the differential kickback noise is significantly improved, because the outputs are separated from the inputs by the input stage. However, this comparator still suffers from high common-mode kickback noise due to the clocked input stage.

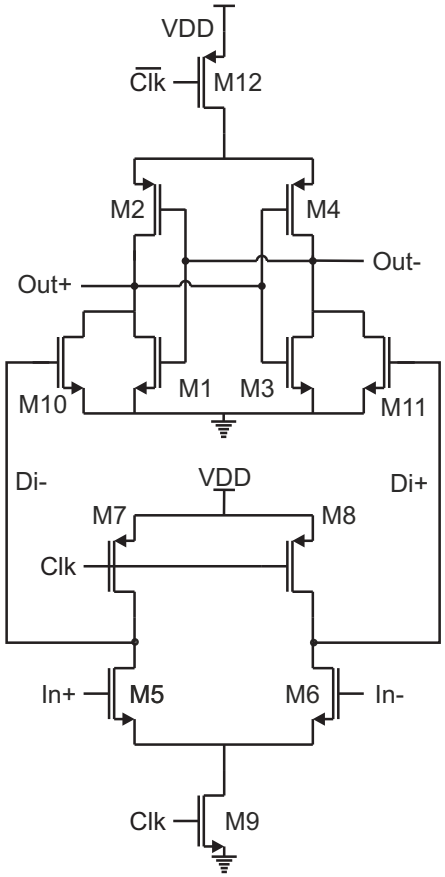

Figure 4.6: Double-tail dynamic latched comparator

4.1.2 Proposed comparator

Regarding the analysis above, reducing the common-mode kickback noise as well as differential kickback noise is the key aim of the novel dynamic latched comparator. Fig. 4.7 shows the circuit of the novel dynamic latched comparator.

Unlike the comparator in Fig. 4.6, the proposed comparator uses only one stage to perform the operation. The input pair is implemented by the common source pair M11 and M12 (CS) [54].

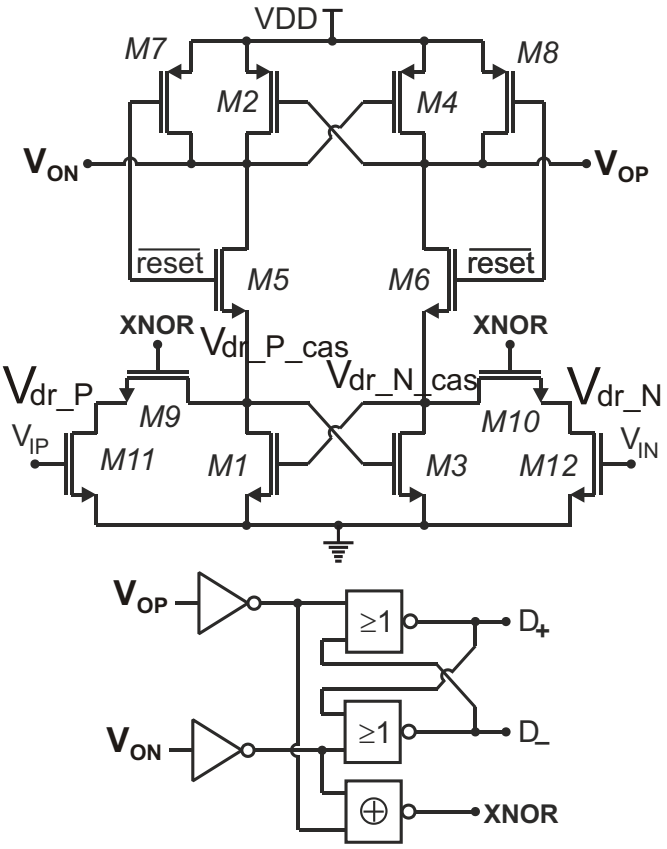

Figure 4.7: Dynamic latched comparator with reduced kickback noise

The input common source transistors sink the current from the regenerative cross-coupled inverters (M1/M2 and M3/M4). In the reset phase ($\overline{\textbf{Reset}}$=0), the PMOS M7 and M8 are switched on, clamping V_{on} and V_{op} to VDD. The switches M9 and M10 are switched on, driven by the XNOR gate, which is controlled by the output signals V_{on} and V_{op}. Once $\overline{\textbf{Reset}}$ goes high during the regeneration phase, the NMOS transistors M5 and M6 are turned on, whereas PMOS transistors M7 and M8 are switched off. So the voltages at V_{on} and V_{op} start falling from VDD. Depending on the current drawn by the CS input pair M11 and M12, the slew rate difference between the falling voltages of V_{on} and V_{op} will be further enlarged by the regenerative cross-coupled pair, until the comparator outputs reach the supply rail voltages.

Compared to the dynamic latched comparators of Fig. 4.5, this comparator produces less common-mode kickback noise. This is due to the use of a common-source input pair, whose gate-source capacitances are always connected to ground. The large voltage switching of source nodes as in many other dynamic latched comparators is thereby avoided. As a result, the common-mode kickback noise caused by the gate-source coupled capacitance is totally suppressed.

Furthermore, the differential kickback noise is also significantly reduced. Just as the voltage difference between V_{op} and V_{on} starts to be enlarged by the positive cross-coupled inverters at the beginning of the regeneration phase, the inverter-buffers connected to V_{op} and V_{on} will amplify the voltages. Thereby the XNOR gate will be triggered by the buffer amplifier and turn off the switches M9 and M10. This leads to a decoupling of the CS input pair from the output nodes V_{op} and V_{on}, before the voltage variation of V_{op} and V_{on} is further enlarged until it reaches the supply rail voltages. Therefore, the differential kickback noise caused by the large variation of output nodes is significantly reduced by the decoupling mechanism of the switches in series to the input transistors.

4.1.3 Verification, comparison and analysis

To demonstrate the advantages of this novel dynamic latched comparator over other dynamic latched comparator, both comparators are simulated under the same conditions. The typical and proposed dynamic latched comparators, which are shown in Fig. 4.5 and Fig. 4.7, are implemented in 0.13 μm CMOS technology. The dimensions for both comparators are defined in Table 4.1 and Table 4.2, respectively.

Table 4.1: Dimensions of typical dynamic latched Comparator in Fig. 4.5

	M1	M2	M3	M4	M5	M6
W (μm)	8	24	8	24	2	2
L (μm)	0.2	0.2	0.2	0.2	0.2	0.2
	M7	M8	M9	M10	M11	
W (μm)	2	2	8	24	24	
L (μm)	0.2	0.2	0.2	0.2	0.2	

The input resistors of 20 kΩ are connected in series with the inputs of both comparators as shown in Fig. 4.8. The resistors simulate the resistance of a V/I

Table 4.2: Dimensions of Proposed Comparator in Fig. 4.7

	M1	M2	M3	M4	M5	M6
W (μm)	8	24	8	24	4	4
L (μm)	0.2	0.2	0.2	0.2	0.2	0.2
	M7	M8	M9	M10	M11	M12
W (μm)	2	2	4	4	24	24
L (μm)	0.2	0.2	0.2	0.2	0.2	0.2

converter connected to I-DAC. At the same supply voltage of 1.5 V the transistors of the input pair, the cross-coupled inverters and the switches in the typical dynamic comparator use the dimensions equal to that defined in the proposed comparator, respectively. Unter the same setup conditions, the performance difference of both comparators will be observed and analyzed in this section.

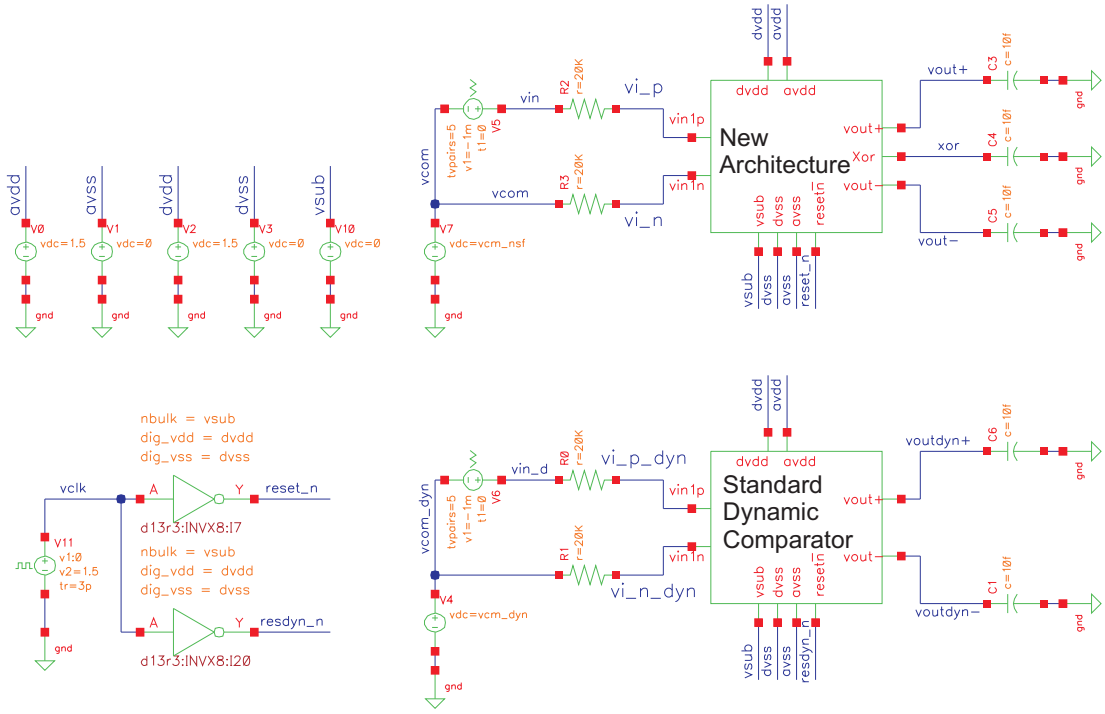

Figure 4.8: Testbench of kickback noise simulation

In Fig. 4.9 the simulation results of a standard dynamic comparator are shown. In the reset phase the D/S nodes V_{Drain_P}/V_{Drain_N} of the input pair are pulled up to VDD of 1.5 V and high potential of about 1 V, respectively. When $\overline{\textbf{Reset}}$ is rising, the voltages of drain and source nodes start falling from 1.5 V and 1 V to ground in the regeneration phase. The large voltage variation produces obviously

high kickback current. In this case, the peak current is about 20 μA, which is measured at the gate of the inputs. Moreover, the most important thing is that

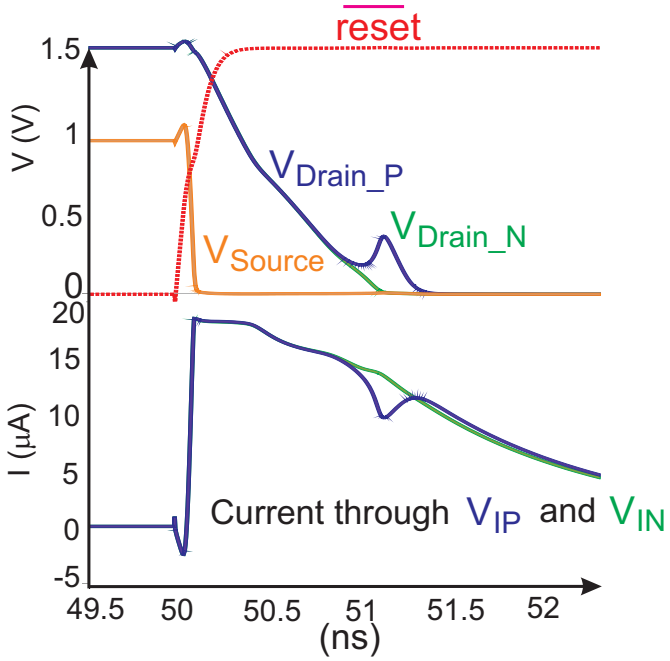

Figure 4.9: Simulation of standard dynamic latched comparator

both currents flow in the same direction. That means the main kickback noise for the dynamic latched comparator comes actually from the common-mode kickback noise instead of differential kickback noise. If the differential kickback noise would be larger than the common-mode kickback noise, the currents should flow in complementary directions, not in the same direction. Of course, the differential kickback noise has also some contributions to the disturbance. However, its peak value is only about 5 μA, which is much less than common-mode kickback noise. Hence we can say that the dynamic latched comparator suffers mainly from the common-mode kickback noise.

In Fig. 4.10 the simulation of the proposed comparator is shown. In the new comparator the kickback noise is significantly improved. As we see, the common-mode kickback noise current is reduced down to 6 μA, which is less than one third of the standard dynamic comparator. And the differential kickback noise current is also reduced to 2.5 μA, which is only the half of the value in the standard comparator.

The reason for the improvement is based on two facts. First of all, the source nodes of the input pair transistors are always connected to ground. Secondly in

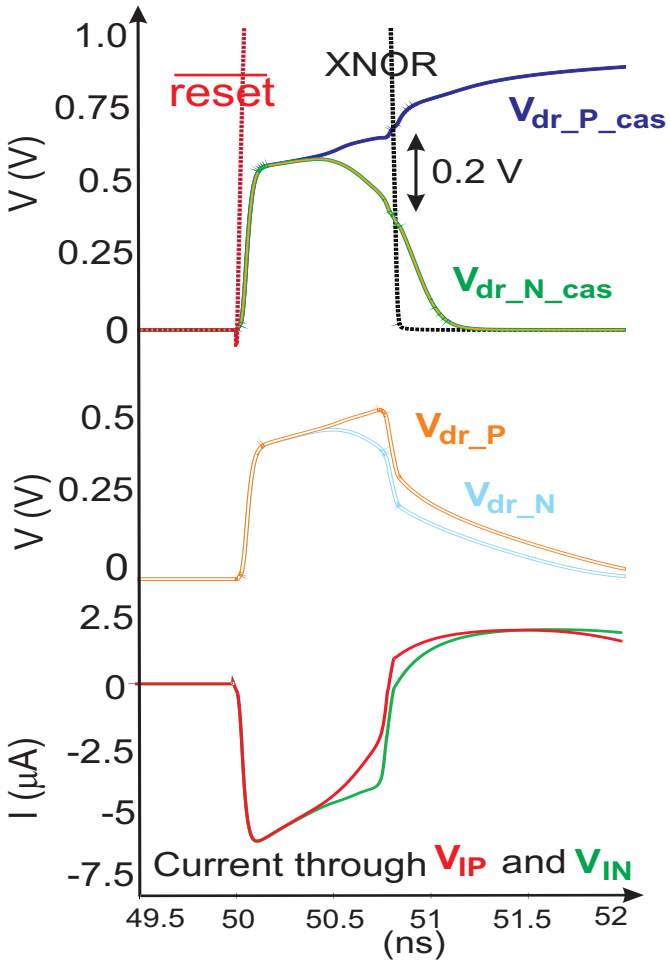

Figure 4.10: Simulation of proposed dynamic latched comparator

the reset phase the drain nodes of the input transistors are set to ground instead of VDD, compared to the standard dynamic comparator. When $\overline{\textbf{Reset}}$ is rising, the voltage step at the drain nodes is limited to 0.5 V.

Furthermore, differential kickback noise is also reduced by a decoupling mechanism. The decoupling mechanism in the proposed comparator is implemented by a self-controlled switching of the transistors M9 and M10. Controlled by the signals V_{on} and V_{op}, the signal XNOR turns the switches M9 and M10 on or off. As shown in Fig. 4.10, just at the time point when the deviation of $V_{dr\_P\_cas}/V_{dr\_N\_cas}$ is raised to 0.2 V, the signal XNOR is already fallen to ground and hence the input pair is decoupled from V_{on} and V_{op}. As a result, the deviation of both kickback noise currents is limited to a peak value of 2.5 μA much less than in the standard comparator. So the differential kickback noise is considerably reduced.

According to the injected currents, the kickback noises of both comparators

measured across an input resistor of 20 kΩ are shown in Fig. 4.11 (a) and (b), respectively. The kickback noise of the proposed comparator is about 120 mV, whereas the noise of the typical dynamic comparator is about 400 mV, which is more than three times of the new architecture.

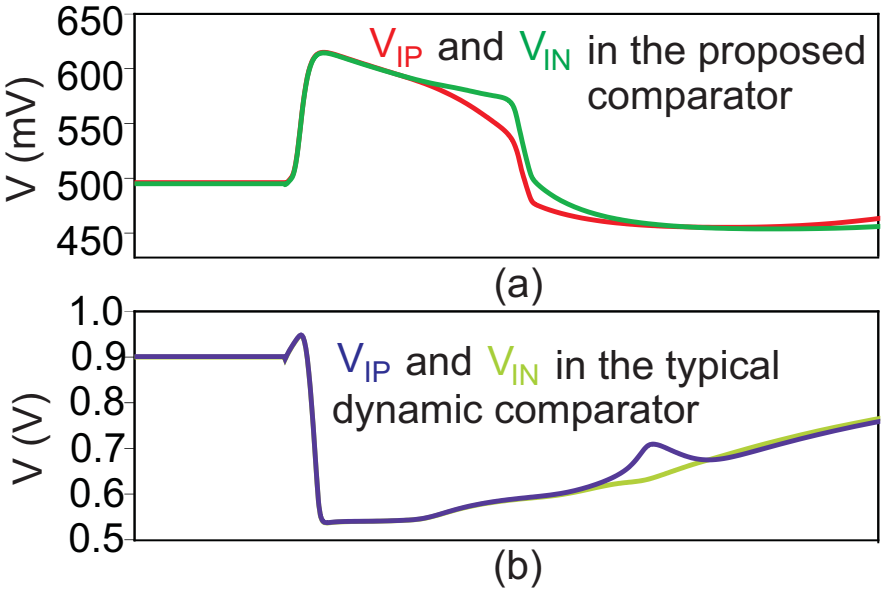

Figure 4.11: Comparisons in terms of kickback noise

4.2 Short settling time

Besides the low kickback noise, the presented comparator performs faster than the standard dynamic latched comparator. This is based upon the common-source input pair transistors, which enhance the input voltage difference of the latch. To determine the short settling time of the proposed comparator, the back-to-back inverters building up the latch stage of dynamic comparators are analyzed in this section. Along with stardard dynamic comparator, a comparison between the proposed and standard dynamic comparator is performed to demonstrate the advantages of the proposed comparator.

A typical latch, which consists of back-to-back inverters, has one metastable state. Without any disturbances and noise, both inverters share the same voltage at their input and output. But in practice thermal noise or parasitic disturbances will trigger the latch to leave its metastable state and enter into one of the latch

states. The time during the state transition from metastability to absolute stability is the settling time of comparator [16].

Based on this analysis, the latch stage is linearized around the DC operating point of the metastable state. Looking at the transistor level, the model of the inverter with its output capacitance, transconductance and output resistance can be simplified to the circuit in Fig. 4.12. The small signal modeling of the latch is derived as shown in Fig. 4.13, where each inverter in the latch is considered as an OTA with the transconductance G_m. C_{ox} represents load and parasitic capacitances at the output.

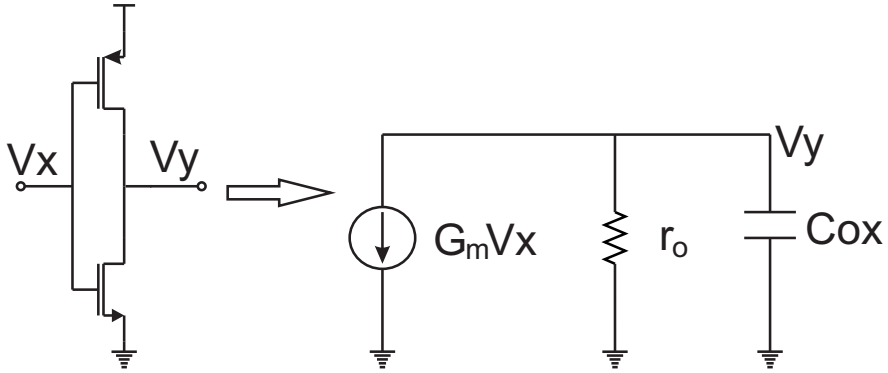

Figure 4.12: Small signal modeling of inverter

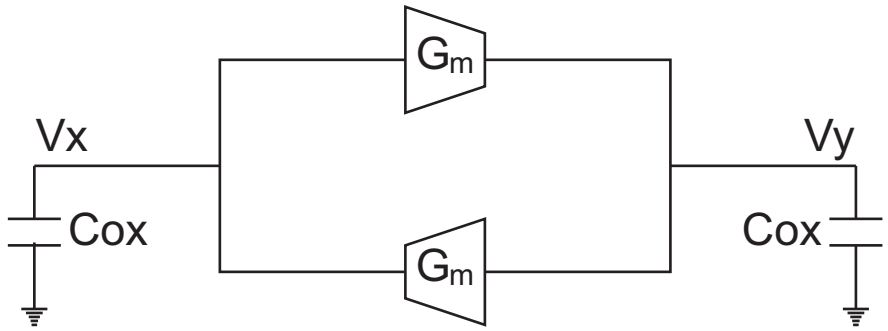

Figure 4.13: Modeling of latch

The sum of the current at each inverter node must be zero:

$$C_{ox} \cdot \frac{\delta V_y}{\delta t} + \frac{V_y}{r_o} + G_m \cdot V_x = 0 \tag{4.2}$$

Considering both inverters together, the first-order differential equations of each

output of latch can be derived as:

$$\begin{aligned} \frac{\delta V_y}{\delta t} + \frac{V_y}{C_{ox} \cdot r_0} &= -\frac{G_m \cdot V_x}{C_{ox}} \\ \frac{\delta V_x}{\delta t} + \frac{V_x}{C_{ox} \cdot r_0} &= -\frac{G_m \cdot V_y}{C_{ox}} \end{aligned} \tag{4.3}$$

Subtracting both equations and assuming that $V_y - V_x = V_D$, the differential output of the latch represented by V_D is expressed as:

$$\begin{aligned} \frac{\delta V_y}{\delta t} - \frac{\delta V_x}{\delta t} &= \frac{\delta \left(V_y - V_x\right)}{\delta t} \\ \frac{\delta V_D}{\delta t} &= V_D \cdot \frac{1 + G_m \cdot r_o}{C_{ox} \cdot r_o} \end{aligned} \tag{4.4}$$

This homogenous differential equations has a solution $V_D = V_{Do} \cdot e^{\lambda \cdot t}$. Rewriting Eq. 4.4 yields:

$$\begin{aligned} V_{Do} \cdot e^{\lambda \cdot t} &= V_{Do} \cdot e^{\lambda \cdot t} \cdot \left(\frac{1 + G_m \cdot r_0}{C_{ox} \cdot r_o}\right) \\ \lambda &= \frac{1 + G_m \cdot r_o}{C_{ox} \cdot r_o} \\ G_m \cdot r_o = A, \text{ if } A \gg 1,\ \lambda &\cong \frac{G_m}{C_{ox}} \end{aligned} \tag{4.5}$$

Therefore, the settling of output voltage of the latch can be described as:

$$V_D\left(t\right) = V_{Do} \cdot e^{t/\tau} \text{ with } \tau = 1/\lambda = \frac{C_{ox}}{G_m} \tag{4.6}$$

Reducing the time constant τ, the settling time of the comparator is decreased. For the standard dynamic latched comparator, $G_m = g_{m\_nch} + g_{m\_pch}$, where g_{m_nch} and g_{m_pch} are transconductances of N-channel and P-channel MOS transistors. Of course, if MOS transistors of the inverters operate in the linear region, their transconductances are different from that of the saturation region. However, in the proposed comparator the common-source input pair operated in the saturation or lineary region always sinks the current from the latch as shown in Fig. 4.14. So the transconductance of common-source input pair is added to G_m of the latch.

$$G_m = g_{m\_nch} + g_{m\_pch} + g_{m\_in} \tag{4.7}$$

As a result, the time constant τ and the settling time is decreased, compared to a typical dynamic latched comparator.

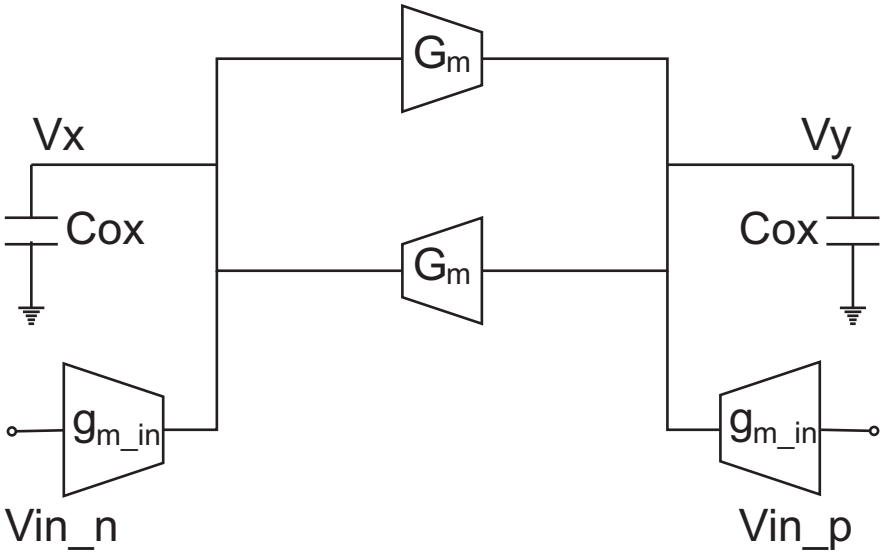

Figure 4.14: Modeling of proposed latch

To verify the settling characteristics, the standard dynamic latched comparator and proposed comparator are simulated under the same condition. The settling of the output voltages (V_{op} and V_{on}) is depicted in Fig. 4.15. The proposed comparator performs about 0.8 ns faster than the standard dynamic comparator, which is a reduction of about 70%. This result confirms that, along with the reduced kickback noise, the proposed comparator operates much faster than the typical dynamic comparator.

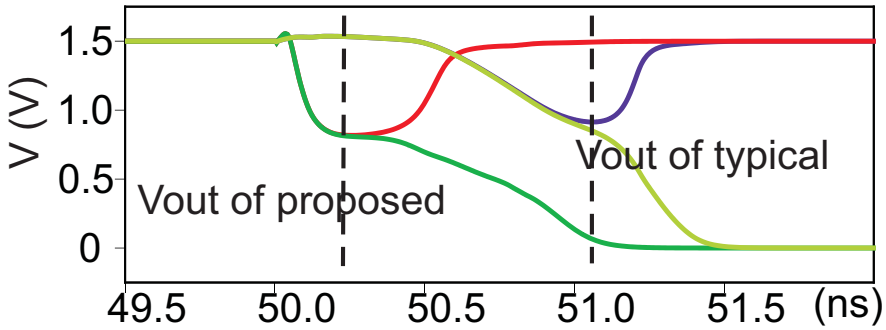

Figure 4.15: Comparison of settling time between dynamic and proposed comparators

4.3 Thermal noise

4.3.1 Analysis

At the switching point, not only kickback noise but also thermal noise may disturb the input signal, leading to decision errors. Especially in high speed comparators thermal noise integrated over a wide frequency range can reach the milivolt range, restricting the resolution of comparator considerably.

In the presented dynamic latched comparator the input-referred thermal noise is reduced by the common-source input pair. As shown in Fig. 4.16 the comparator is split symmetrically in two parts, which can be analyzed independently. The drain of the CS input transistor depicted in the dashed frame is connected to the output of inverter. At the cross point of metastablity , where the latch has the highest sensitivity to noise, the thermal noise current ($\overline{I^2_{inv}}$) generated from one inverter in the latch is added to the CS input transistor V_{in_p} in the small signal model.

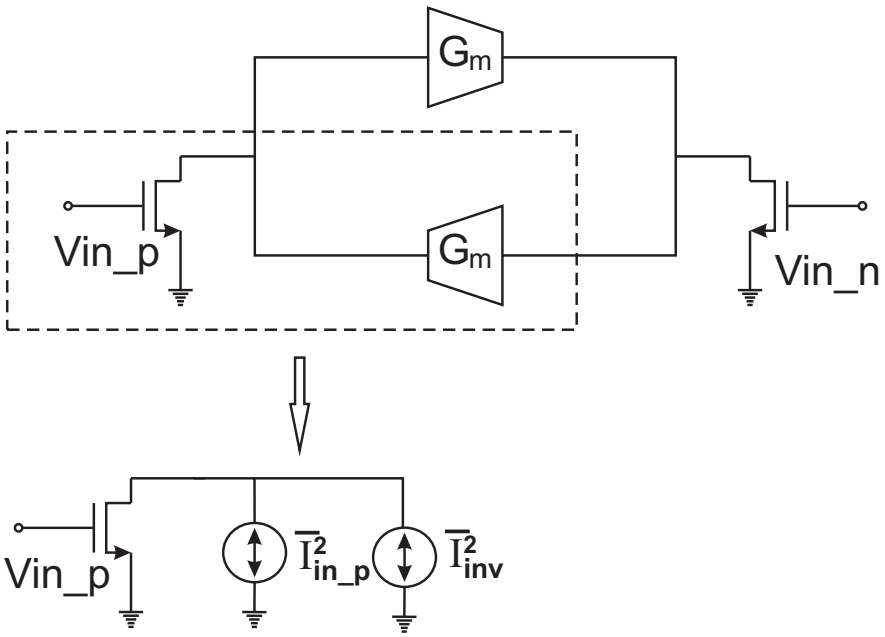

Figure 4.16: Thermal noise reduction

The noise current of the CS input transistor $\overline{I^2_{in\_p}}$ is in parallel to the inverter thermal noise $\overline{I^2_{inv}}$. The input-referred thermal noise voltage can be derived by

dividing the noise current with the transconductance of the CS input:

$$Var(V_{in\_p}) = \overline{V_{noise}^2} = \frac{\overline{I_{in\_p}^2} + \overline{I_{inv}^2}}{g_m^2} \tag{4.8}$$

However, this input-referred noise voltage is referred to ground and is not a differential noise voltage between V_{in_p} and V_{in_n}. Due to the fact that the noise is described by power or variance, the differential noise power between both inputs is described as:

$$Var(V_{in\_p} - V_{in\_n}) = Var(V_{in\_p}) + Var(V_{in\_n}) \tag{4.9}$$

Combining both equations, the variance of the differential noise referred to the inputs is:

$$\begin{aligned} Var(V_{in\_p} - V_{in\_n}) &= Var(V_{in\_p}) + Var(V_{in\_n}) \\ &= 2 \cdot \left(\frac{\overline{I_{in\_p}^2} + \overline{I_{inv}^2}}{g_m^2} \right) \end{aligned} \tag{4.10}$$

As discussed in the section 2.2, the noise current of MOS transistors is proportional to its transconductance [15, 16, 21]. So applying Eq. 2.9, the differential noise is derived and described in detail as:

$$\begin{aligned} Var(V_{in\_p} - V_{in\_n}) &= 2 \cdot \left(\frac{4k_BT \cdot G_m + 4k_BT \cdot g_m}{g_m^2} \right) \\ &= 2 \cdot \left(\frac{4k_BT \cdot G_m}{g_m^2} + \frac{4k_BT}{g_m} \right) \end{aligned} \tag{4.11}$$

where G_m and g_m represent the transconductances of each inverter in the latch and the common source input transistor, respectively.

Obviously, the direct and simplest approach for reducing the input-referred thermal noise is to increase the g_m of input transistor and decrease the G_m of inverter in the latch. But the settling time of the latch as discussed above is inversely proportional to the transconductance of latch. So a trade-off is required. If we consider Eq. 4.11, it can be seen that the noise depends on the relative ratio between G_m to g_m, whereas the time constant of the latch is related only to the total transconductance of the latch. It is noted that the whole transconductance of latch in our comparator includes not only the G_m of the inverter but also the g_m of input transistor. If we can increase the g_m of the input transistor to compensate the decreased G_m of the inverter, the increased g_m of the input

transistor can further reduce the input-referred thermal noise, at the same time the requirement for a short settling time is also included.

An optimum design of the latch uses the same short channel NMOS and PMOS transistors. Additionally, the larger g_m of input CS transistor relative to the latch transistors are preferred to be chosen for the reduction of input-referred thermal noise. The input transistors use the same channel length as in the inverter of the latch. The channel width of input transistors is so defined that its g_m is two times of the value of G_m of the inverters. As a result, the input-referred thermal noise generated by the latch is roughly reduced to 1/4, compared to the standard dynamic latched comparator.

4.3.2 Noise modeling

The traditional approach of noise exploration is based on the DC operating point. The thermal noise generated by MOS transistor depends on the operation mode of saturation or linear. The thermal noise and 1/f noise of MOS transistor depend on this operation mode.

For the analysis of thermal noise characteristics of MOS transistors, we can consider the voltage of the latch at the metastable cross point. But to obtain more precise data of noise characteristics, the typical noise simulation techniques upon the DC operating point is not accurate enough. Therefore, the approach of transient noise simulation, which is usable in clocked comparators with non-linear characteristics, is applied to check the influence of thermal noise during the latch operation.

All simulations including transient noise simulation are based on the BSIM4 transistor model. However, the transient noise model provided by TSMC's 130 nm technology does not work properly. Fig. 4.17 shows the test bench of a N-channel transistor, which operates in the saturation region. The drain current depicted as **MOS-Ids** is directly measured and copied by the instance of **VMids**, which is implemented by the cell of **Vdc** in the library of Cadence. The drain current of this MOS transistor is verified by AC-noise as well as transient noise simulation. The left diagramm in Fig. 4.18 shows a thermal noise level of AC simulation of $1.63 \cdot 10^{-21} \mathrm{A}^2/\mathrm{Hz}$, matching the theoretical value of $\overline{i^2_{noise}} = 4k_BT \cdot g_m$, with a g_m of the NMOS transistor of 163 mS. But the transient noise simulation deviates significantly from the theoretical value and the AC noise simulation as reference simulation under the same conditions. The value of transient noise simulation

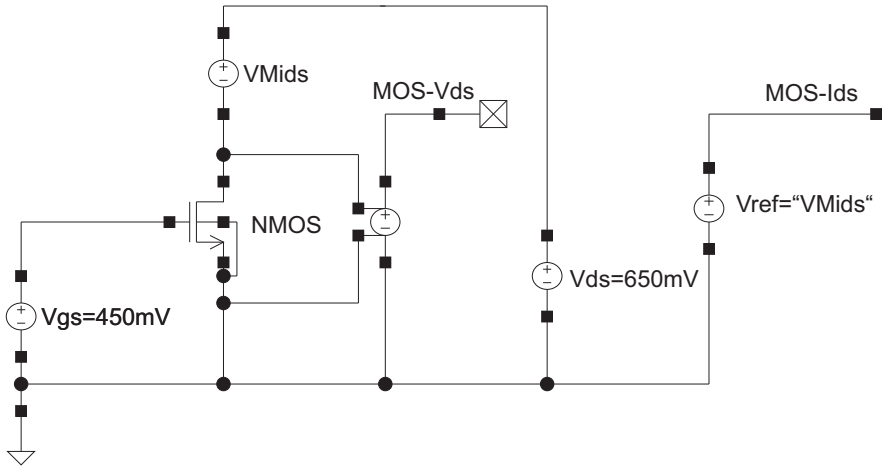

Figure 4.17: Testbench for noise simulation of N-channel transistor

is about 4 orders lower than the expected value. Therefore, additional noise sources are designed individually and specifically for each transistor of this latched comparator.

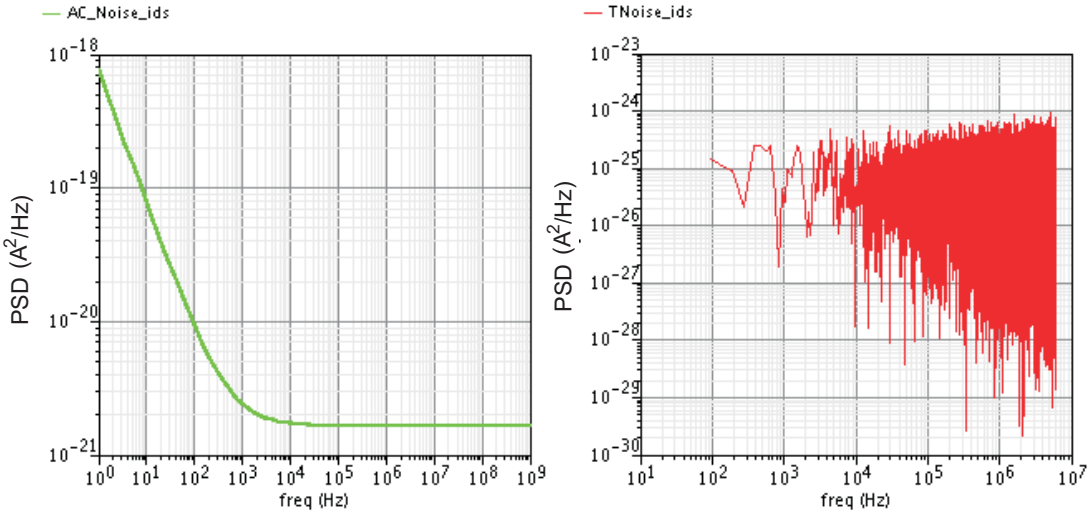

Figure 4.18: Comparison of correct AC-and wrong transient-noise model

The basic solution for the wrong model is shown in Fig. 4.19. One extra noise current source is added in parallel to the MOS transistor. This current source is determined by the operation region of the transistor, e.g., saturation, linear or sub-threshold region.

The noise current source comprises three functional blocks. There are the noise currents for the linear and the saturation regions as shown in Fig. 4.20

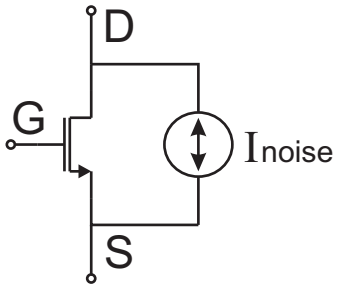

Figure 4.19: Basic principle

and Fig. 4.21, and the multiplexer in Fig. 4.22, which selects the noise source, according to the operation region.

1) Noise model for the linear region

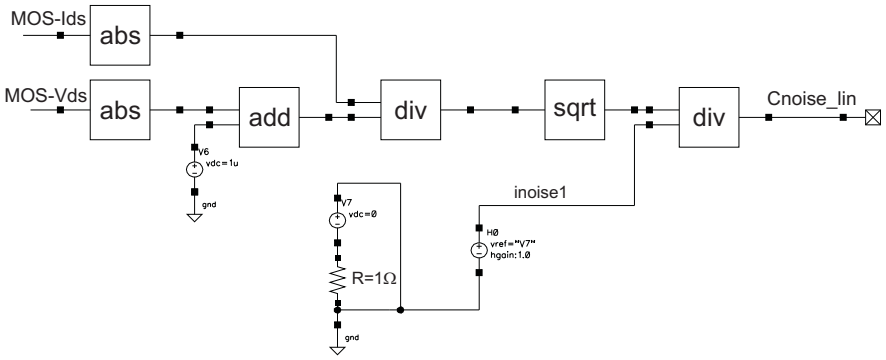

Figure 4.20: Noise current source in linear region

If the MOS transistor works in the linear with $V_{ds} \leq V_{gs} - V_{TH}$, the channel resistance is:

$$r_{lin} = \frac{V_{ds}}{I_{ds}} \tag{4.12}$$

So the signals of **MOS-Vds** and **MOS-Ids** of Fig. 4.17 are selected and divided to calculate the conductance $1/r_{lin}$. As the PSD of the noise current is inversely proportional to the channel resistance as:

$$\overline{I_n^2} = 4k_BT \cdot 1/r_{lin}, \tag{4.13}$$

the conductance is further multiplied with the unit noise current of **inoise1** of the model to create the thermal noise in the linear region. In addition, some AHDL modules are added to avoid signal overflow and convergence problems. At the voltage nodes 1 MΩ resistors are added, but in its edition option "generation

noise" is turned off. (Otherwise, these resistors would produce more noise than the MOS transistor of the model.)

2) Noise model for the saturation region

Like the noise of the linear region, the PSD of the noise current in the saturation region is proportional to g_m, which is:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_{ds}} = \alpha \cdot \sqrt{I_{ds}} \tag{4.14}$$

Eq. 4.14 gives not an exact number at small transistor geometries. Therefore, to match the noise characteristics, the factor α must be fitted to the AC simulations results. Fig. 4.21 shows the circuit for noise generation in saturation region.

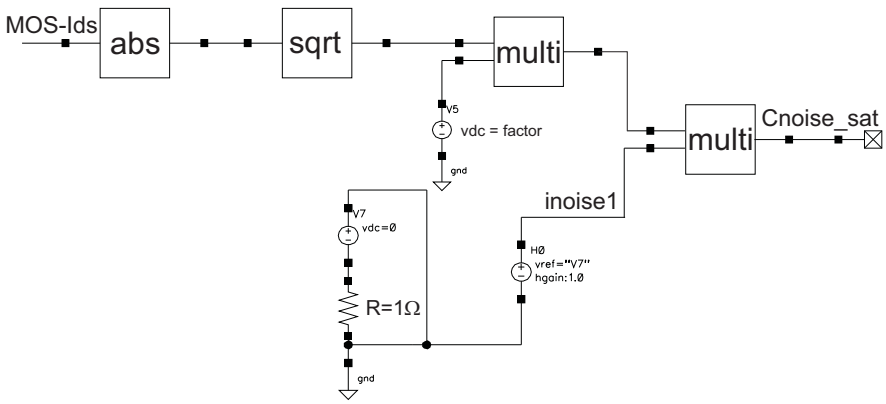

Figure 4.21: Noise current source in saturation region

3) Multiplexer for noise source selection

Because the DC operating point of the latched comparator changes continuously over time, a multiplexer for selection of the noise source is needed. The basic selection criterion is the comparison of the effective voltage of $(V_{gs} - V_{TH})$ to V_{ds}. When the effective voltage is greater than the drain-source voltage, the noise source for linear region is selected. Otherwise, the noise source of the saturation is transferred to the MOS transistor. The noise source of the saturation region is used for subthreshold as well. Fig. 4.22 presents the multiplexer concretely.

Using the described additional noise generator, the model is extended and the transient noise simulation produces sensible and appropriate result as seen in Fig. 4.23. The operators used in the noise model are provided by EDA-tool Cadence.

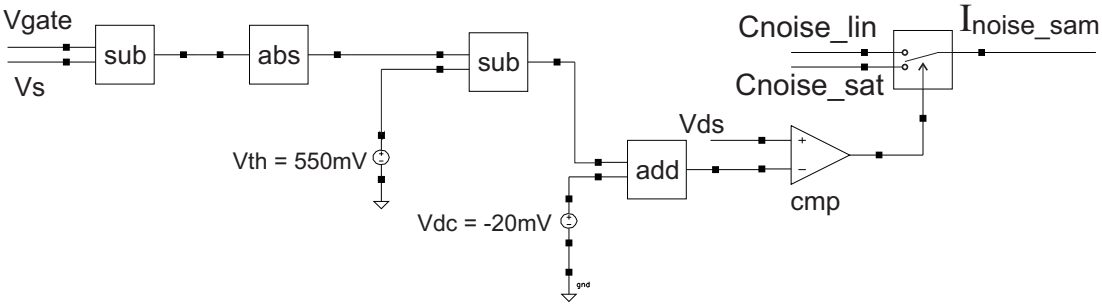

Figure 4.22: Selection of noise current source

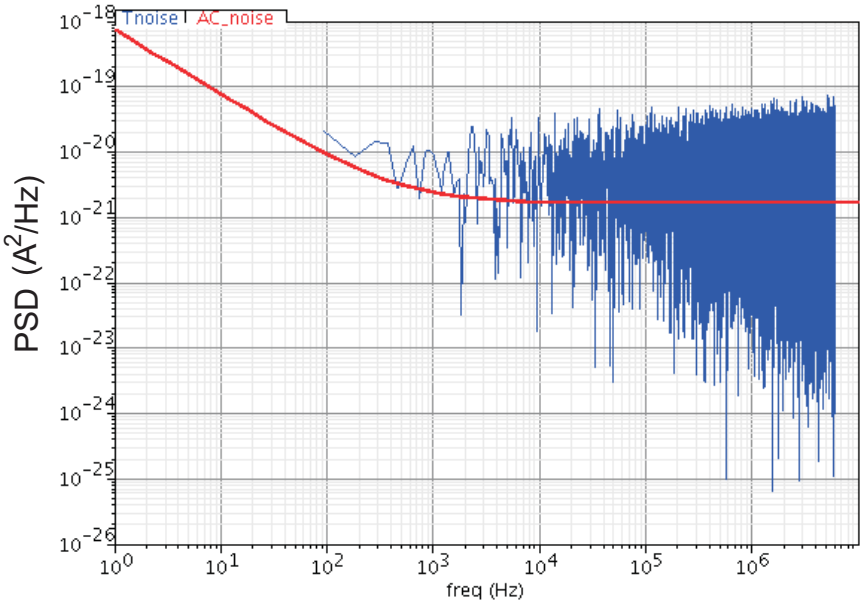

Figure 4.23: Comparison of AC and Tansient noise simulation

4.3.3 Verification

In a latched comparator, which exposes the characteristics of non-linearity, a transient noise simulation is an adequate approach for the verification of thermal noise. But because of a wrong MOS noise model, an additional noise generator is used as described in section 4.3.2.

It may look unusual that the noise generator is connected to the drain of the MOS transistor as seen in Fig. 4.24. The reason is that the drain of MOS transistors is the output. If the noise appears at the drain of the MOS transistor, which feeds or sinks the current from other connected transistors, the noise at the drain of the MOS transistor will affect the circuit.

Obviously not all of the transistors in our proposed latched comparator have

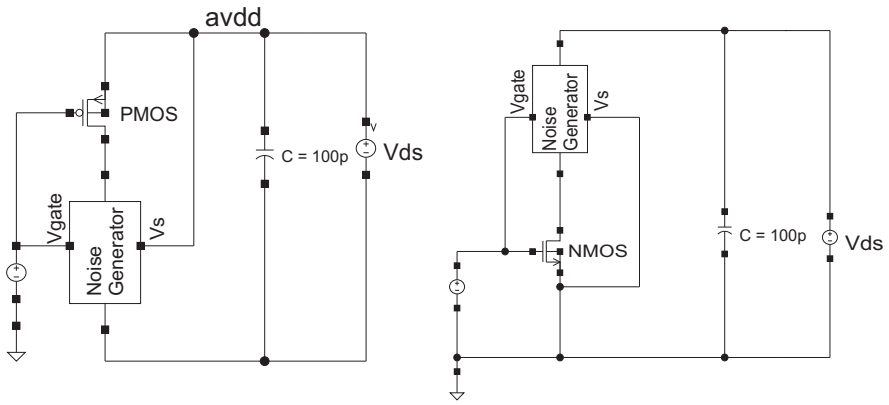

Figure 4.24: Test bench of single MOS transistor for transient noise simulation

the source nodes connected to the analog ground as seen in Fig. 4.25. Nevertheless, the noise generators are anyway connected to the transistors M5/M6 and M9/M10 as we mentioned above, because the thermal noise generated by M5/M6 and M9/M10 has a minimum impact to our comparator. The transistors M5/M6 and M9/M10 operate in this comparator as switches, which are either on or off. If in the off-state, the comparator is in reset mode. In the on-state the switches operate as cascode. In this case the on-resistance of the switches is minimum, generating low thermal noise, which can be neglected.

In our design, the transient noise simulation setting is in Table 4.3:

Table 4.3: Setup of transient noise simulation

Stop time	60n
Accuracy	conservative
Noise Fmax	50G
Noise Seed	1
factor	2
Skipcount	20

The simulations show that the noise disturbs the operation of the latched comparator, especially when the input difference is smaller than 640 μV. To illustrate the impact of thermal noise on the operation of the latched comparator, a transient simulations with an input signal difference equal to 300 μV is depicted in Fig. 4.26. The outputs of the latched comparator (D−/+) are instable, stepping up and down randomly. Consequently, the input-referred thermal noise for a yielding better than 99.7% for 6-sigma standard must be reduced to 3.6 mV,

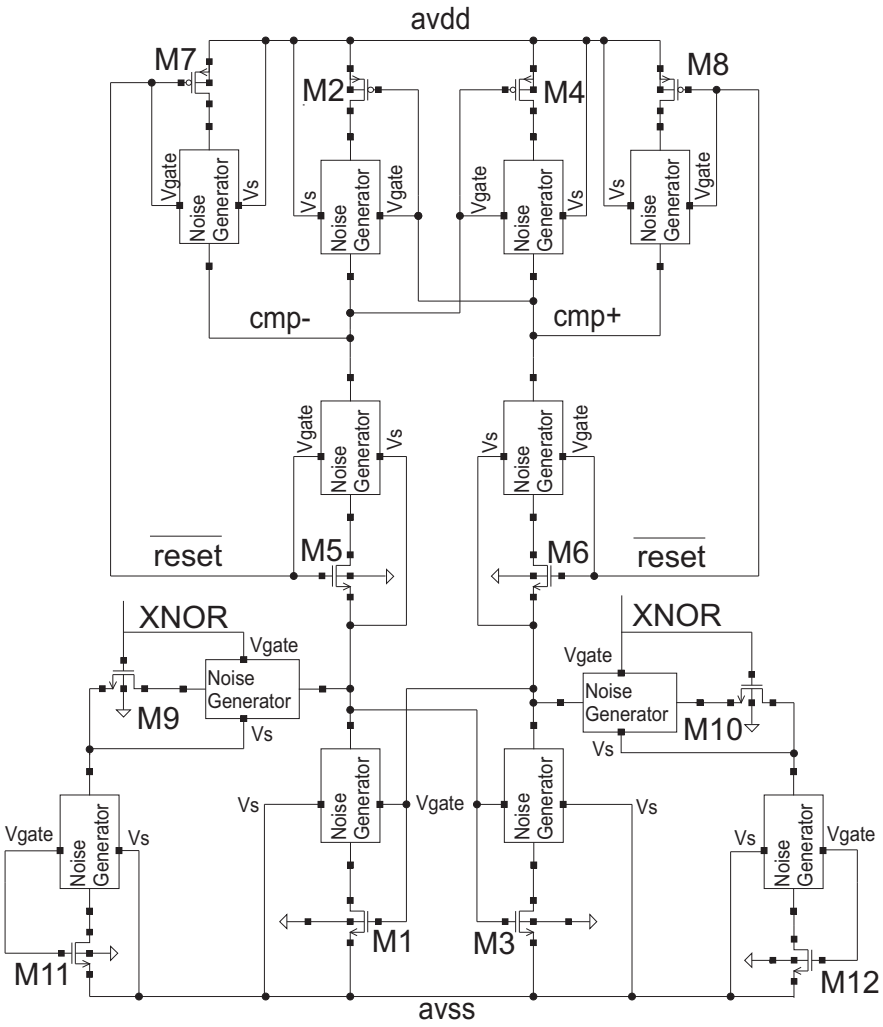

Figure 4.25: Test bench of latched comparator for transient noise simulation

which is smaller than the LSB voltage of 5 mV. Therefore, the input-referred thermal noise has minimal influence to our comparator.

Until now the input-referred DC offset voltage is not discussed specifically in this work. As mentioned in section 2.3.1.1 the DC offset voltage does not limit the performance of the latched comparator as well as the ADC, because in the system level this type of errors can be digitally corrected and calibrated. But to get a first impression of how large the DC offset voltage could be in this comparator, Monte Carlo simulations are applied to explore the characteristics of DC offset caused by mismatch of transistors. Fig. 4.27 shows the result of a Monte Carlo simulation with 620 runs. It is seen that the input-referred DC offset voltage in this work is less than 1 mV, which corresponds to the standard deviation of less

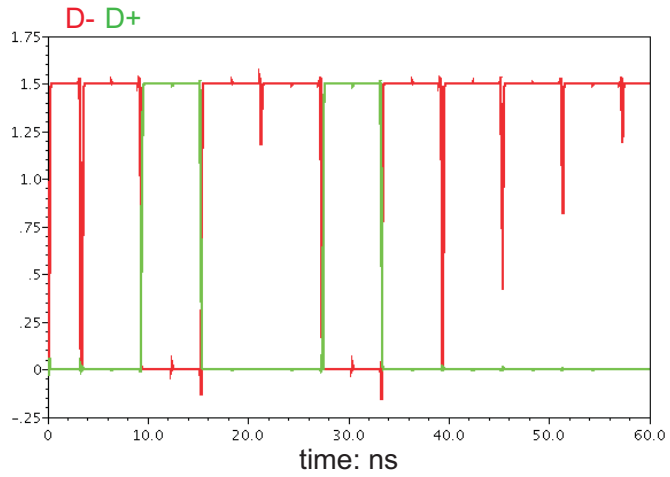

Figure 4.26: Noise simulation with differential input equal to 300 μV

than 0.2 mV, if 6-sigma standard deviation is used in this case. It is good result for a comparator with very small dimensions, but it must be mentioned that Monte Carlo simulation can deviate from practical results. Hence, it is strong recommended to use a calibration system for offset error correction.

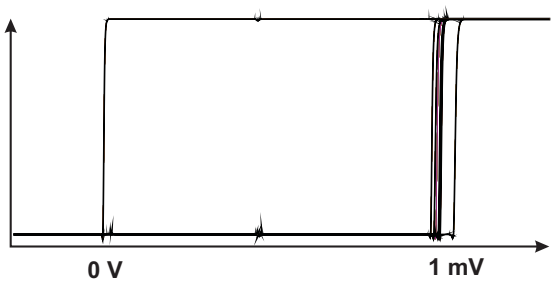

Figure 4.27: Offset simulations (620 Monte Carlo runs)

4.4 Comparator performance summary

In this chapter a new type of comparator design with reduced kickback noise is presented and its functionality is demonstrated. It is confirmed that the common-mode kickback noise is the predominant kickback noise source in standard dynamic comparators.

The CS input stage of the new latched comparator has much lower common-mode kickback noise. The automatic decoupling mechanism reduces differential kickback noise and prohibits static current consumption, achieving high power efficiency. In the realized comparator the peak noise is reduced down to 120 mV

if measured across an input resistor of 20 kΩ. This value is much smaller than the value presented in [54] (with 1 kΩ). The differential kickback noise currents are also reduced down to the half of a standard dynamic comparator.

The proposed comparator performs faster than the standard dynamic latched comparator. This is due to two factors: The first is, this comparator uses only three transistor in stack instead of 4 transistor as in [49]. The second is the additional CS input stage. By using the CS input stage the difference of voltage slew rate of the latch is enhanced, because the CS input transistors sink additional currents from the output capacitances and discharge them faster. At a clock frequency of 1 GHz this comparator consumes 0.75 mW, which is lower than in previous publications of [55, 56]. Additionally, the input-referred thermal noise is also reduced by the CS input stage down to 3.6 mV, which is smaller than the LSB voltage of 5 mV in this ADC.

With respect to the characteristics including power efficiency, kickback noise and thermal noise, this dynamic latch comparator exposes its excellent advantages, which could be used in applications, where high power efficiency and low noise disturbance are required. Table 4.4 summarizes the performance of the presented comparator.

Table 4.4: Summary of Proposed Comparator Characteristics

Technology	130	nm
Input resistance	20	kΩ
Injected current	6	μA
Common-mode kickback voltage	120	mV
Sampling frequency	1	GHz
Power dissipation	0.75	mW
Input-referred thermal noise	0.6	mV
DC static offset	1	mV

Chapter 5

ADC design

This chapter describes the integration of the new comparator with other components on the ADC. Before we go into details, it must be mentioned that signals inside the core circuit of the ADC do not always directly match the requirements of a practical application, especially the voltage levels of digital input and output. Therefore, some peripheral circuits are used on the chip, for instance, IO-buffer driver, clamp and ESD-diode, to interconnect the core circuit with the application system.

In this book the main purpose is to introduce the reader the new operation principle of the ADC with respect to the application in power management. Hence, to facilitate the reader to understand the working principle of this ADC, we focus on the main functional blocks or core circuits.

5.1 Voltage-to-current converter

The voltage-to-current converter (VIC) is simply realized using a 20 kΩ resistor. Among the voltage to current converters recently published in the literature [57, 58], all of them use the feedback control mechanism to achieve a high linearity. But the signal bandwidth of the feedback amplifier limits the conversion speed, resulting in a longer settling time. Additionally the output of the VIC is connected to the I-DAC, which has a high output resistance. Even under small process variations and mismatch appearing in the feedback path of the circuit, a high linearity of the voltage to current conversion can not be guaranteed. Consequently, the small deviations of the converted current produce large voltage errors through the high output of I-DAC.

Compared to the available approaches mentioned [57, 58], the advantages of the principle used here are: First of all, using a resistance allows a high linearity without any difficulties of calibration. It is known that the resistor value suffers from the process variations. These variations cause a deviation of the LSB voltage from its design value, if we assume that the current source of a unit LSB is still constant. But by using a resistor correlated with the unit current source generator, the deviation of the LSB voltage can be precisely calibrated as shown in Fig. 5.1.

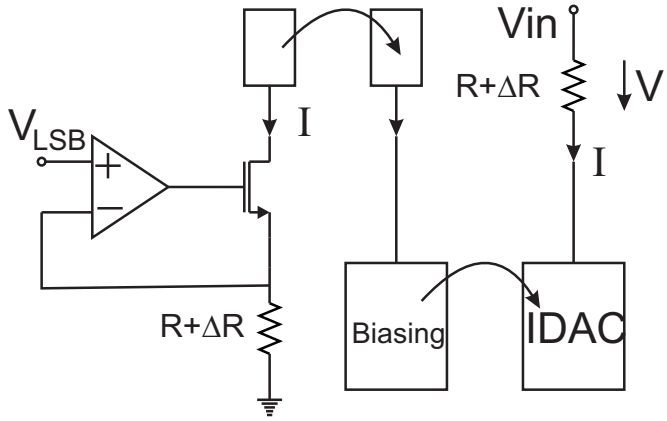

Figure 5.1: Resistance-correlated calibration system

The unit current source of the I-DAC is generated by using a reference resistor. It is assumed that the reference resistor is equal to the input resistor. In the layout both resistors are placed close to each other to achieve good matching. When the variation of the resistance is about ΔR, the current is:

$$I = \frac{V_{LSB}}{R + \Delta R}$$

Mirroring the current from the bias circuit to the I-DAC, the voltage drop across the input resistor is

$$\begin{aligned} V &= \frac{I}{R + \Delta R} \\ &= \frac{V_{LSB}}{R + \Delta R} \cdot (R + \Delta R) \\ &= V_{LSB} \end{aligned} \tag{5.1}$$

It is seen that the mismatch of the input resistance is completely calibrated and the voltage of the LSB in Eq. 5.1 is kept constant by the resistance-correlated current source.

In addition to a simple calibration of mismatch, the bandwidth of the VIC is increased by the input resistance. The converted current through the VIC will be compared with the current of the I-DAC. The residual current between the the VIC and the I-DAC after subtraction will produce a voltage variation across the output resistance. But a high gain due to high load resistance requires a trade-off regarding speed. By using a resistance of 20 kΩ the bandwidth is increased by the relative small resistance. Of course, the voltage gain is reduced, but this does not matter as far as the LSB voltage of 5 mV can be clearly detected by the comparators (see comparator noise chapter 4).

Using just a resistor as VIC is a simple solution, but it has been proven as a practical solution for the single-ended input. Also this solution allows adjustment of reference current to fit different applications.

5.2 Current steering DAC and counter

The threshold voltage of a MOS transistors is not fully scaled with the supply voltage, limiting the dynamic range. To avoid this limitation, the current is chosen as a reference signal in the feedback loop of the proposed ADC.

A current steering DAC is frequently used in applications, where high linearity and low cost are required. Compared to other DACs such as capacitive ones, the silicon area of a current steering DAC is much smaller. Based on these advantages, the current steering DAC is applied in this work.

5.2.1 Review of current steering DAC architectures

The current steering DAC is realized by an array of current sources that are connected in parallel as three types of topologies, namely the binary, unary and segmented architectures [59]. Each of them has its own advantages. Hereby we review the characteristics of these topologies in terms of mismatching and linearity.

In the binary architecture each current source has binary-weighted values of the LSB with binary scaling. The digital input switches directly the current source. Due to the mismatching effects the linearity is limited. Especially in the worst case where a transition occurs at mid-scale, the DNL of the binary scaled

architectures is

$$\begin{aligned} \sigma_{DNL}^2 &= \overbrace{\left(2^{B-1}\right)\sigma_{LSB}^2}^{1000\cdots} + \overbrace{\left(2^{B-1}-1\right)\sigma_{LSB}^2}^{0111\cdots} \\ &= \left(2^B-1\right)\sigma_{LSB}^2 \\ \sigma_{DNL} &= \sqrt{2^B-1}\sigma_{LSB} \end{aligned} \tag{5.2}$$

where B is the resolution of DAC and σ is the standard deviation.

Compared to the binary architecture, the unary architecture shows better performance of DNL, which is written as:

$$\sigma_{DNL} = \sigma_{LSB} \tag{5.3}$$

The reason is based upon the fact that in the unary topology the unit LSB current sources are positioned individually and separately. For the transition at the mid-scale from $0111\cdots$ to $1000\cdots$ only one LSB unit current must be switched on, not as in the binary structure where the MSB current is switched on and all other sources are switched off. Furthermore, a decoder from binary to thermometer code in the unary architecture is required for the control of the individual current sources.

In contrast to the DNL characteristics of binary and unary architectures, the INLs of both structures show the same characteristics as:

$$\begin{aligned} \sigma_{INL}^2 &= \overbrace{\left(2^{B-1}\right)\sigma_{LSB}^2}^{1000\cdots} \\ \sigma_{INL} &= \sqrt{2^{B-1}}\sigma_{LSB} \end{aligned} \tag{5.4}$$

This is because the INL describes the deviation of a DAC between the ideal and actual values, whereas the DNL expresses the difference between two adjacent values.

Segmented architecture combines the characteristics of binary and unary structures, and makes a compromise in terms of DNL. In other words, the DNL of segmented architecture is better than the DNL defined by a binary-weighted converter but worse than the DNL achieved by the unary architecture [59, 60].

The characteristics of high linearity including INL as well as DNL are required in this work. So the unary architecture is chosen to implement the current steering DAC.

5.2.2 Proposed current steering DAC

The current steering DAC [61, 62] in this work consists of 64 well-matched unit current sources. Each unit source is 250 nA, resulting in a maximum current of 16 μA if all I-DAC sources are switched on. This architecture produces a very small DNL error as mentioned above and guarantees a monotone behavior, which is important for the control loop. A possible disadvantage is its INL error. In addition the layout of an unary architecture is more complex due to the wiring to the binary-to-thermometer decoder.

An INL error is mainly caused by process mismatching and variation. Eq. 5.4 describes the INL theoretically, but it is not accurate enough for industrial applications, when a high INL yielding is required. According to a recent publication [63], Eq. 5.4 is modified and derived as:

$$\frac{\sigma_{LSB}}{I_{LSB}} = \frac{1}{2C\sqrt{2^B}} \tag{5.5}$$

Constant C is set to 2.97 for an INL yield better than 99.7%, and B is equal to 6, which represents the resolution of the presented ADC. Therefore, the required standard deviation of the unit current source should be smaller than 5.26 nA.

The current steering DAC has high requirement regarding the matching of MOS transistors. In section 2.2.6 deviations caused by process mismatch have been discussed. Now we want to explore how these deviations impact the characteristics of the I-DAC current source.

For a MOS transistor in saturation region the drain current is

$$I_D = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)\cdot\left(V_{gs}-V_{TH}\right)^2 \tag{5.6}$$

If the parameters μ, W, L and V_{TH} change due to process varition, the drain current change will be

$$\Delta I_D = \frac{\delta I_D}{\delta\left(\frac{W}{L}\right)}\cdot\Delta\left(\frac{W}{L}\right) + \frac{\delta I_D}{\delta\left(V_{gs}-V_{TH}\right)}\cdot\Delta\left(V_{gs}-V_{TH}\right) \tag{5.7}$$

So

$$\frac{\Delta I_D}{I_D} = \frac{\Delta\left(\frac{W}{L}\right)}{\frac{W}{L}} - \frac{2\Delta V_{TH}}{V_{gs}-V_{TH}} \tag{5.8}$$

The parameter W, L, even μ are included in β, so Eq. 5.8 can be simplified:

$$\frac{\sigma^2\left(\Delta I\right)}{I^2} = \frac{\sigma^2\left(\Delta\beta\right)}{\beta^2} + \frac{4\sigma^2\left(\Delta V_{TH}\right)}{\left(V_{gs}-V_{TH}\right)^2} \tag{5.9}$$

Replacing the variance with Eq. 2.12 and Eq. 2.13, the relation between the dimensions of a MOS transistor and the random parameter can be expressed as:

$$(WL)_{min} = \frac{1}{2}\left[A_\beta^2 + \frac{4 \cdot A_{VTH}^2}{(V_{gs} - V_{TH})^2}\right] / \left(\frac{\sigma_{LSB}}{I_{LSB}}\right)^2 \tag{5.10}$$

A_β and A_{VTH} are technology parameters for the mismatch and (V_{gs}-V_{TH}) is the gate overdrive voltage of the unit current source.

From Eq. 5.10 it can be observed that by increasing the (V_{gs}-V_{TH}) the minimum dimension of a unit current source transistor can be decreased, resulting in less gate capacitance, which is important for speed and stability. In accordance to Eq. 5.5 and Eq. 5.10, a current source transistor with a channel length of 13 μm and a channel width of 1 μm is derived by all constraints.

In the practical implementation of the current source a cascode transistor is added in series to the drain as seen in Fig. 5.2. With the isolation of the cascode

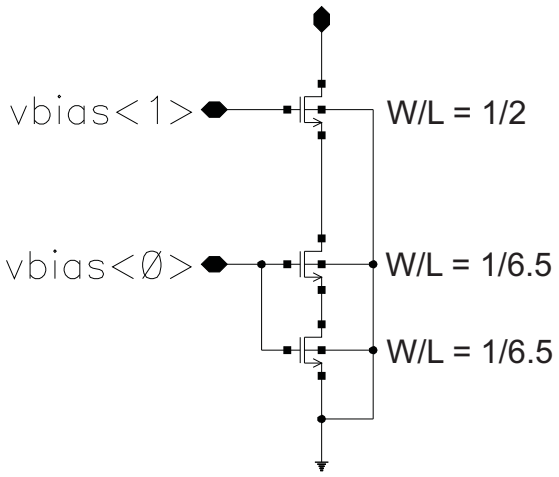

Figure 5.2: Unit current source in I-DAC

transistor the channel modulation effect will be effectively reduced. The voltages of vbias⟨1⟩ and vbias⟨0⟩ are provided by a bias circuit shown in Fig. 5.3, which mirrors the current defined externally exactly to the current source of I-DAC. In this work the wide-swing current mirror is used to bias the unit current source of I-DAC. The unit current source can be adjusted from 100 nA to 400 nA. Its default value is set to 250 nA. Due to this small size, which is very difficult to be applied on the PCB test board, the dimension of cascode MOS transistors in the biasing circuit is scaled by a factor of 8. So the external input current for the biasing circuit is 2 μA. The dimensions of MOS transistors in Fig. 5.3 is depicted

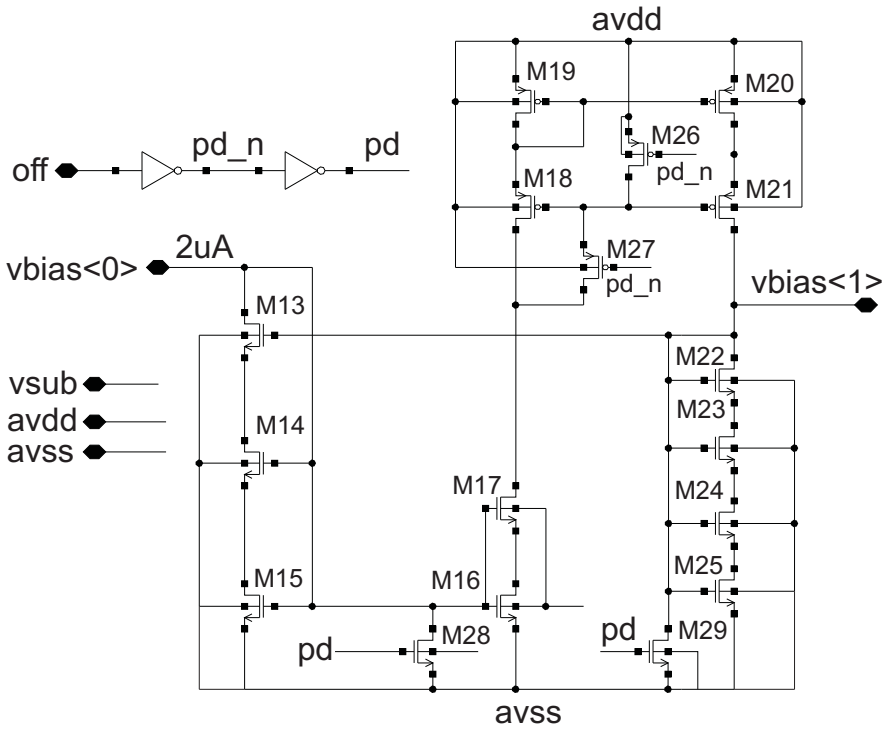

Figure 5.3: Biasing circuit for IDAC

in Table 5.1

The verification of random characteristics of I-DAC is performed by Monte Carlo simulation. The simulated standard deviation shown in Fig. 5.4 is 5.21 nA. Regarding the design value of 250 nA, this current deviation fulfills the requirement of the INL of the I-DAC.

Table 5.1: Dimensions of biasing circuit

	M13	M14	M15	M16	M17	M18
W (μm)	8	8	8	1	1	3
L (μm)	2	6.5	6.5	6.5	6.5	1
	M19	M20	M21	M22	M23	M24
W (μm)	3	3	3	0.4	0.4	0.4
L (μm)	1	1	1	5	5	5
	M25	M26	M27	M28	M29	
W (μm)	0.4	0.3	0.3	0.5	0.5	
L (μm)	5	0.3	0.3	1	1	

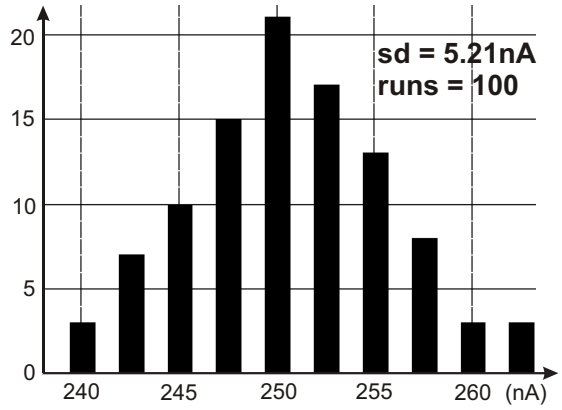

Figure 5.4: Standard deviation of unit current source in Monte Carlo simulation

5.2.3 Thermometer-coded counter

The unit current sources of the I-DAC are controlled by a thermometer-coded counter as shown in Fig. 5.5. The counter is based on a serial shift register, and each output of the shift register is connected to the switch of a unit current source in the I-DAC. The control logic receives the outputs Rdy and Q from the main comparator. Both signals operate inside the counter as clock (Clk) and up-down control (Up/Down) respectively (see Fig. 3.4). The data input Q is sampled and shifted from left to right at the rising edge of the delayed ready-signal Rdy. The individual unit sources of the I-DAC are switched incrementally according to the outputs of the flip-flops of the register.

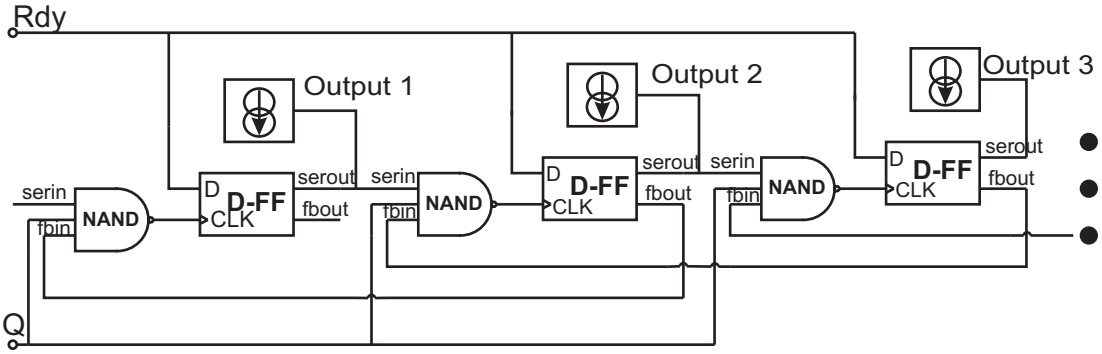

Figure 5.5: Section of thermometer coded shift register

To minimize the propagation delay time of the shift register, one shift register and one unit current source are merged together to one unit cell, as shown in Fig. 5.6. All of 64 unit cells are interlinked and cascaded as shown in Fig. 5.7.

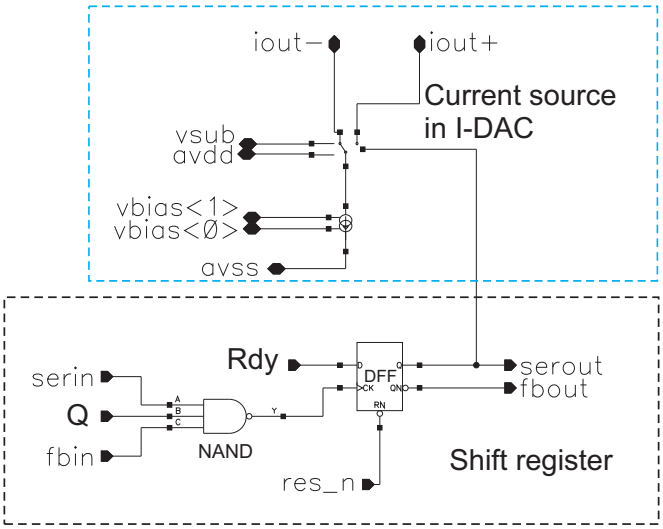

Figure 5.6: I-DAC unit cell including current source and shift register

The layout consists of 2 rows of unit cells with 32 unit cells in each row. The analog sections of the unit cells with a separate analog supply rail are placed at the inner side of both rows, the digital sections of the units are placed at the outside and have a separate digital supply rail, so that the disturbance from digital power supply is isolated from the sensitive analog parts.

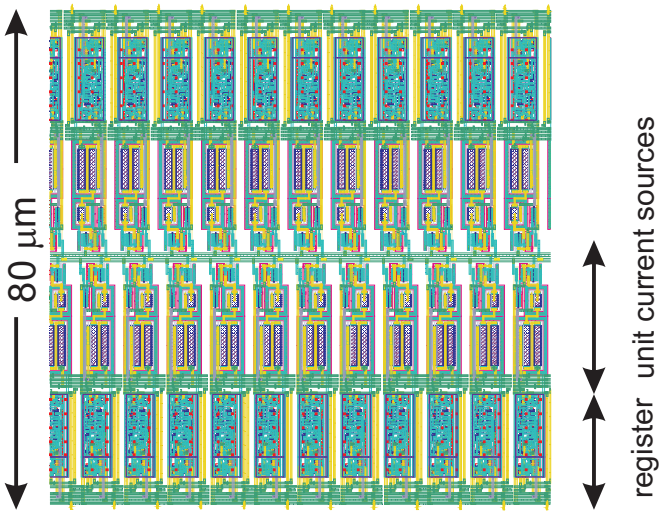

Figure 5.7: Detail of the layout of I-DAC and counter

5.3 Threshold window

A threshold window is used to detect the tracking error and to determine direction and distance of error. If the tracking error exceeds the defined threshold voltage level, the conversion rate of the Tracking ADC will be increased to improve the tracking fidelity at input overlaod.

To implement the mechanism of a threshold window, some ideas have been developed and recently published in [64, 47]. They use double capacitive DACs and double continuous comparators with class-A amplifiers. As mentioned in section 4.1.1 the class-A amplifier has the worst power efficiency. A capacitive DAC can achieve better matching characteristics, if the capacitors are realized as MiM or PiP capacitance. However, neither MiM capacitances nor PiP capacitances are area-saving. So a double capacitive DAC occupies large silicon area.

In this work a new design idea has been developed to solve these issues. For each data conversion only the main comparator and one of both auxiliary comparators is chosen to be triggered. Hence we can say that regarding the signal comparison actually two comparators are applied in the operation in terms of power dissipation. Furthermore, two auxiliary comparators are used to define and create the operational range of a threshold window. The auxiliary comparators use the same architecture as the main comparator, the only difference is that there are programmable resistors inserted to the source followers as depicted in Fig. 5.8.

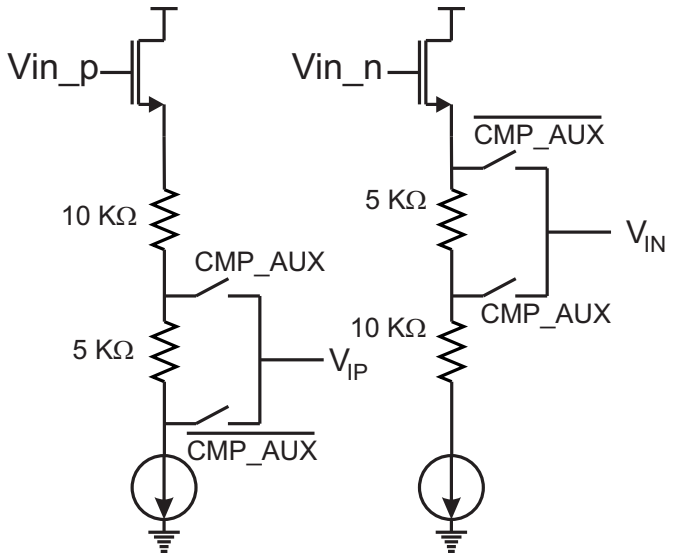

Figure 5.8: Threshold window creation

The bias currents of both source followers are set to 2 μA. With series resistances of 10 kΩ and 5 kΩ, the differential offset voltages are defined as 30 mV and 10 mV respectively, depending on the selection of signal CMP_AUX. If CMP_AUX is logic high, an offset voltage of 30 mV is selected. Otherwise, an offset voltage of 10 mV is chosen. Although the serial resistors limit the bandwidth of the source follower, it still achieves a gain-bandwidth-product (GBW) of 0.6 GHz, still fulfilling the specification. Fig. 5.9 and Fig. 5.10 show the simulation results.

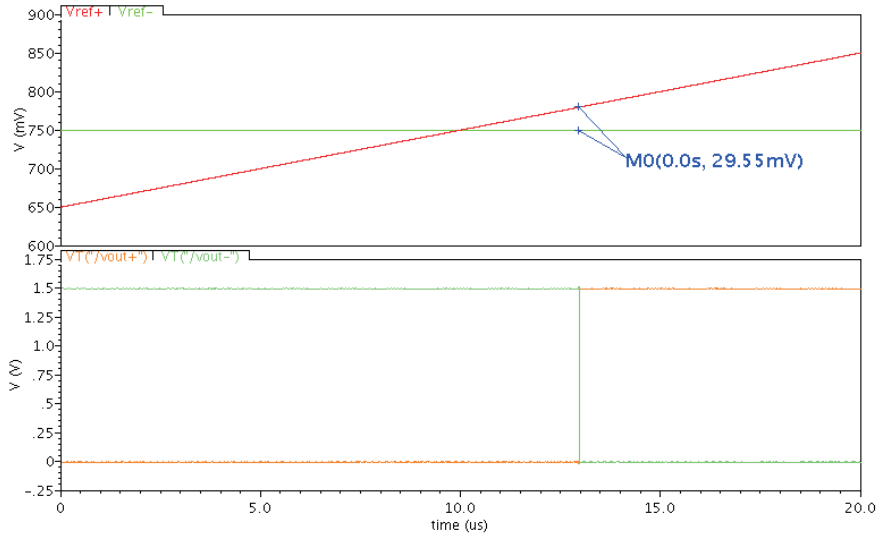

Figure 5.9: Offset voltage of 30 mV for the threshold window

5.4 Digital Control

In Fig. 3.4 all of the digital signals associated with the clock generation and control are part of digital control block. In this section we will describe in detail the digital control block and demonstrate how the digital control block operates and controls the timing of the other blocks.

5.4.1 Architecture and signal flow

Fig. 5.11 shows the detailed digital control block, which comprises the fast/slow mode, the mode selection and the block of clock trigger. **Cmp** and **CmpRdy** are outputs of the main comparator and are connected without any delay to the

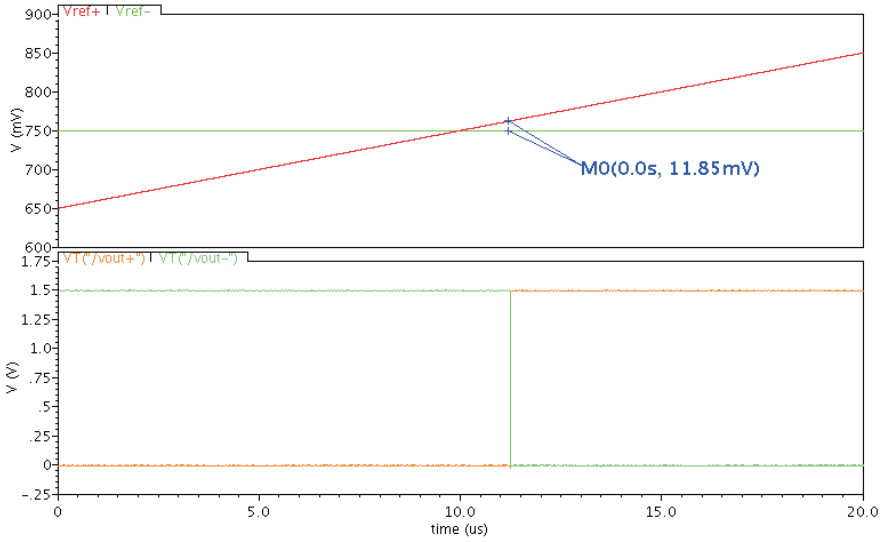

Figure 5.10: Offset voltage of 10 mV for the threshold window

inputs of the counter controlling I-DAC. The reset signal to the main comparator and auxiliary comparators comes from the output **Res** of the digital control block. **Aux_Cmp1** and **Aux_Cmp2** are the output signals from the auxiliary comparators. According to the values of **CmpRdy** and the outputs of the auxiliary comparators, one of mode "fast" and "slow" will be selected by the mode selection block. The delayed elements in the mode setting facilitate a clock of 50 MHz and 12.5 MHz, respectively. Furthermore, a Return-to-Zero signal **R2Z** used as the input of the clock trigger block captures the delayed **CmpRdy** and produces the reset **Res** for the comparators initiating a new operation cycle.

The signal flow of the digital control block is displayed in Fig. 5.12. Initially the reset signal **Res** is set to logic high to trigger the main comparator. Once the comparison is settled, the ready-signal **CmpRdy** is set to logic high (**CmpRdy**=1). Through the delay path of fast or slow mode state, the **CmpRdy** signal is passed through the clock trigger block to signal **R2Z**. Subsequently, the clock trigger block inverts the **R2Z** signal and set the **Res** to be logic low, resetting the main comparator. Once the main comparator is reset by **Res**, the **CmpRdy** of the main comparator is forced to be logic low right now (**CmpRdy**=0). Similar to **CmpRdy**=1, the logic low of **CmpRdy** will be delayed also through the delay elements of fast or slow mode. When the **CmpRdy** as "**R2Z**" arrives at the block of clock trigger, signal **Res** with a logic high is produced this time, starting a new clock cycle.

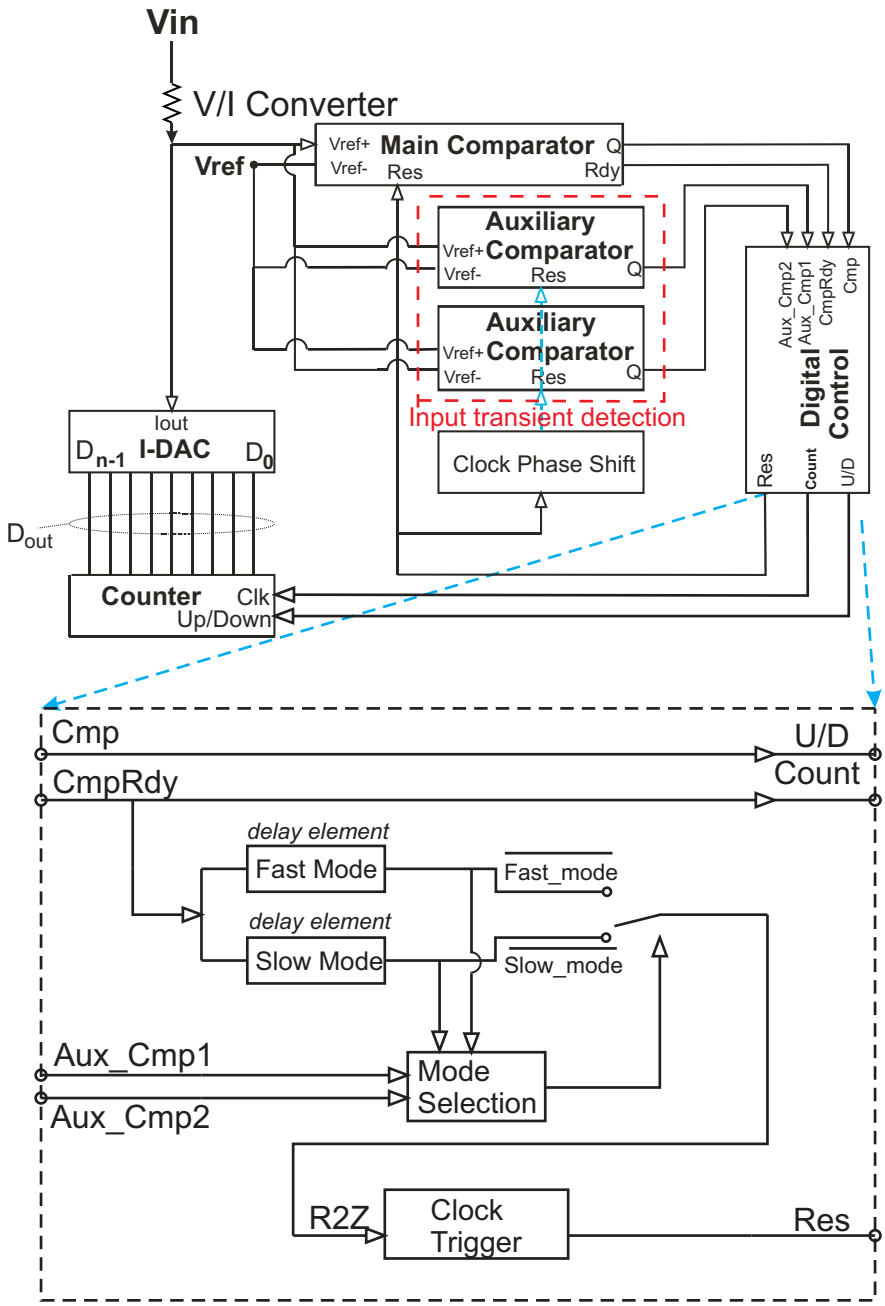

Figure 5.11: Functional block of digital control

5.4.2 Implementation

In this work the fast and slow modes are implemented by an inverters' chain in Fig. 5.13. Both delay modes share the same unit delay inverter, so the number of unit delay inverter of the slow mode is 4-times the fast mode. In order to reduce the power consumption of delay modes, the number of unit inverter could be re-

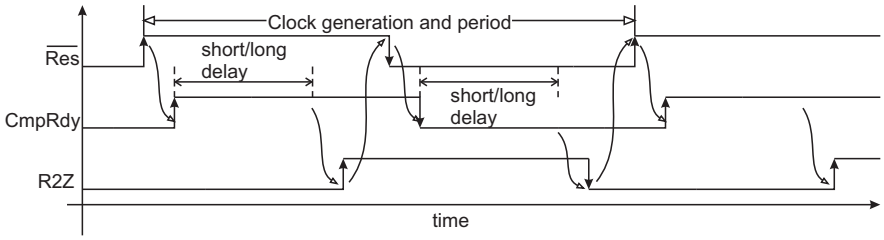

Figure 5.12: Signal flow of digital control block

duced by increasing the channel length of MOS transistors. When the delay time of each unit inverter is increased, the number of unit inverters is correspondingly decreased for the given delay time.

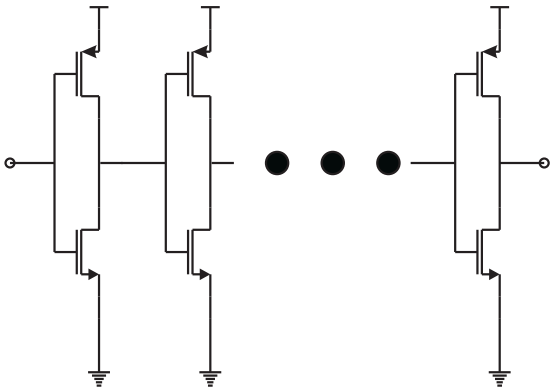

Figure 5.13: Dealy path implementation of fast and slow modes

The mode selection block, which selects the signal **CmpRdy** from the fast and slow mode delay elements, works principlly as a multiplexer. But the multiplexer cannot be realized by pure logic. If so, any time just as one output of both auxiliary comparators is logic high, the current delay mode will be abruptly switched. So the current clock period would be forcefully interrupted to resume the new clock period. As a result, the undesirable spike at the feedback as well as the output of ADC will be seen. Therefore, a D-FF register is used to synchronize the mode switching with the comparator reset phase (Fig. 5.14).

The D-FF register is used to sample and hold the control signal during the current clock cycle. The clock pin **clk** of the D-FF determines the switching point of the delay mode. If a mode switching is required, it must be done at the beginning of a new comparator period. Therefore, the $\overline{\mathbf{Res}}$ signal is fed back to the AND gate in the mode selection block to enable the transition between the delay modes. The OR gate connected to **Aux_Cmp1** and **Aux_Cmp2** detects

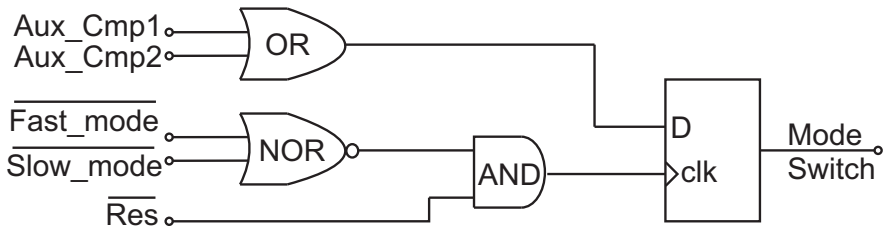

Figure 5.14: Implementation of mode selection

an exceeding tracking error, while the NOR gate ensures the delayed signals in the fast and slow modes to be in the same phase. Therefore, only when $\overline{\textbf{Res}}$ is rising, and $\overline{\textbf{Fast\_mode}}$ and $\overline{\textbf{Slow\_mode}}$ are both logic low, the OR-catenation of **Aux_Cmp1** and **Aux_Cmp2** is sampled by the D-FF, performing the operation of the mode switch.

Basically the clock trigger block works as an inverter. But the circuit in Fig. 5.15 must also initialize the system with an external reset **"Reset_n"**. As **Reset_n** is logic low, the whole ADC is reset. When **Reset_n** is rising, the asynchronous feedback loop is activated and the self-clocking states is running.

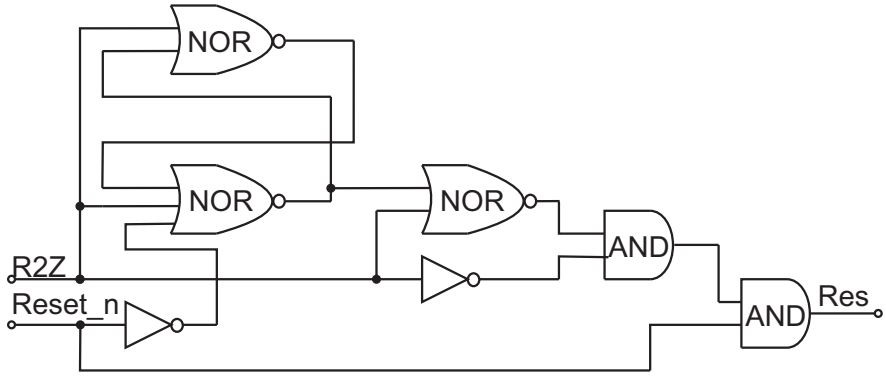

Figure 5.15: Implementation of clock trigger

5.5 Clock phase shift

A clock phase shifter is used to activate the main and auxiliary comparators that operate in the complementary phases. This reduces the interference between comparators due to high kickback noise. For instance, if the main comparator is regenerated at the rising clock edge, the auxiliary comparators are just being reset at the falling clock of **Aux_res**.

Furthermore, the power dissipation of auxiliary comparators can be reduced by conditionally switching the auxiliary comparator. In Fig. 5.16 the signal flow is presented. At the left side the clock (**Main_Res**) and output (**Main_Cmp**) of main comparator as well as the clock (**Aux_Res**) of the auxiliary comparators are depicted. At the right side the threshold window is shown. If the decision of

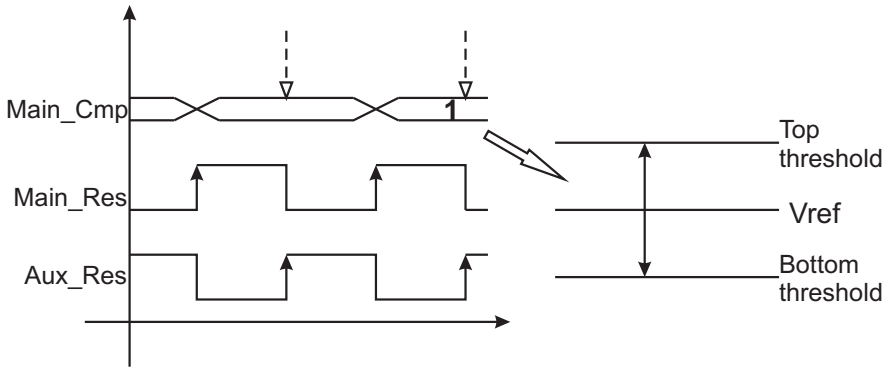

Figure 5.16: Signal flow of clock phase shift

main comparator is logic high, only the upper auxiliary comparator for the high-threshold must be triggered, because the input signal is deviating away from the reference voltage, staying in the region of the top threshold. Otherwise, the lower auxiliary comparator for the low-threshold must be triggered.

By using the clock phase shifter always one auxiliary comparator is activated, while another is kept reset. Thus, the power dissipation of one auxilary comparator is reduced by the multiplexed phase shifter shown in Fig. 5.17.

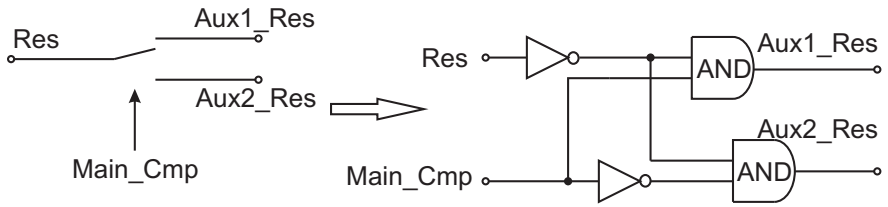

Figure 5.17: Phase shifter of clock trigger

Chapter 6

Experimental measurement

6.1 Layout and packaging

The proposed ADC, which is described in the precedent chapters, is implemented and fabricated on TSMC 130 nm single-Poly, six-Metal (1P6M) low power CMOS technology. The top-level schematic and layout of the proposed ADC including the pads and IO cells are shown in Fig. 6.1 and Fig. 6.2, respectively.

The dimension of the core is about $200\times400\,\mu m^2$, while this whole test chip occupies $1087\times798\,\mu m^2$. The minimum pad opening is $40\,\mu$m and the pitch is $70\,\mu$m. The chip micrograph of this ADC is shown in Fig. 6.3.

Based on the process parameters of TSMC technology, this ADC is bonded and assembled in the MQFN package of 32 pins with the cavity size of $3403 \times 3403\,\mu m^2$. The bonding diagram with the defined pins of this ADC is shown in Fig. 6.4 and Table 6.1.

This ADC is normally operated in the self-clocked mode or asynchronous mode. Keeping the concept of design for test (DFT), some pins must be added in the chip to evaluate its performance. Specifically for the characteristics of linearity this ADC must be clocked and measured in the synchronous mode by the test equipments. Thus, the pins such as CLK_IN, CTRL_SW, SYN_CLK and SYN_MOD are used to switch the operation of the ADC between synchronous and asynchronous modes.

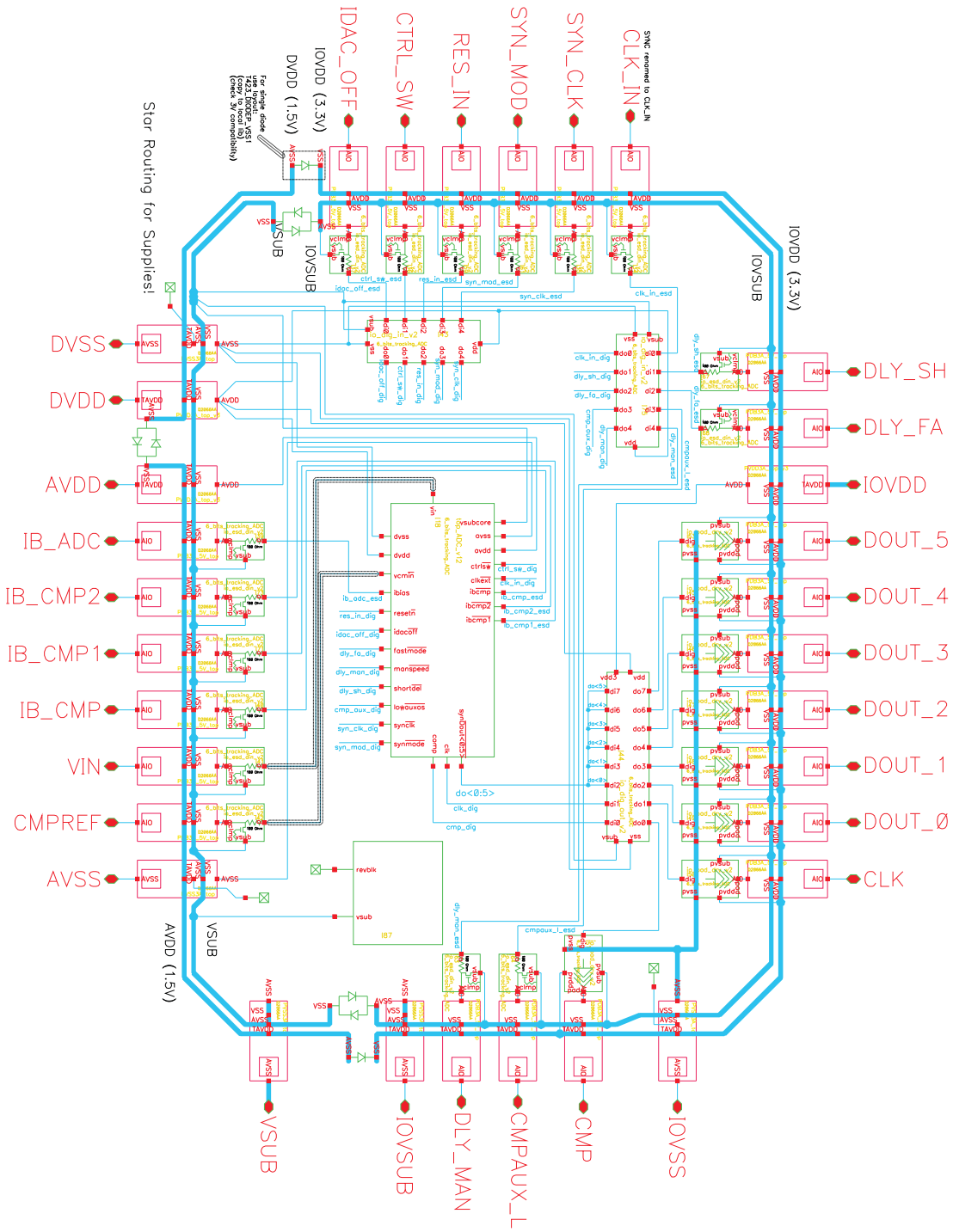

Figure 6.1: Top level of the presented ADC

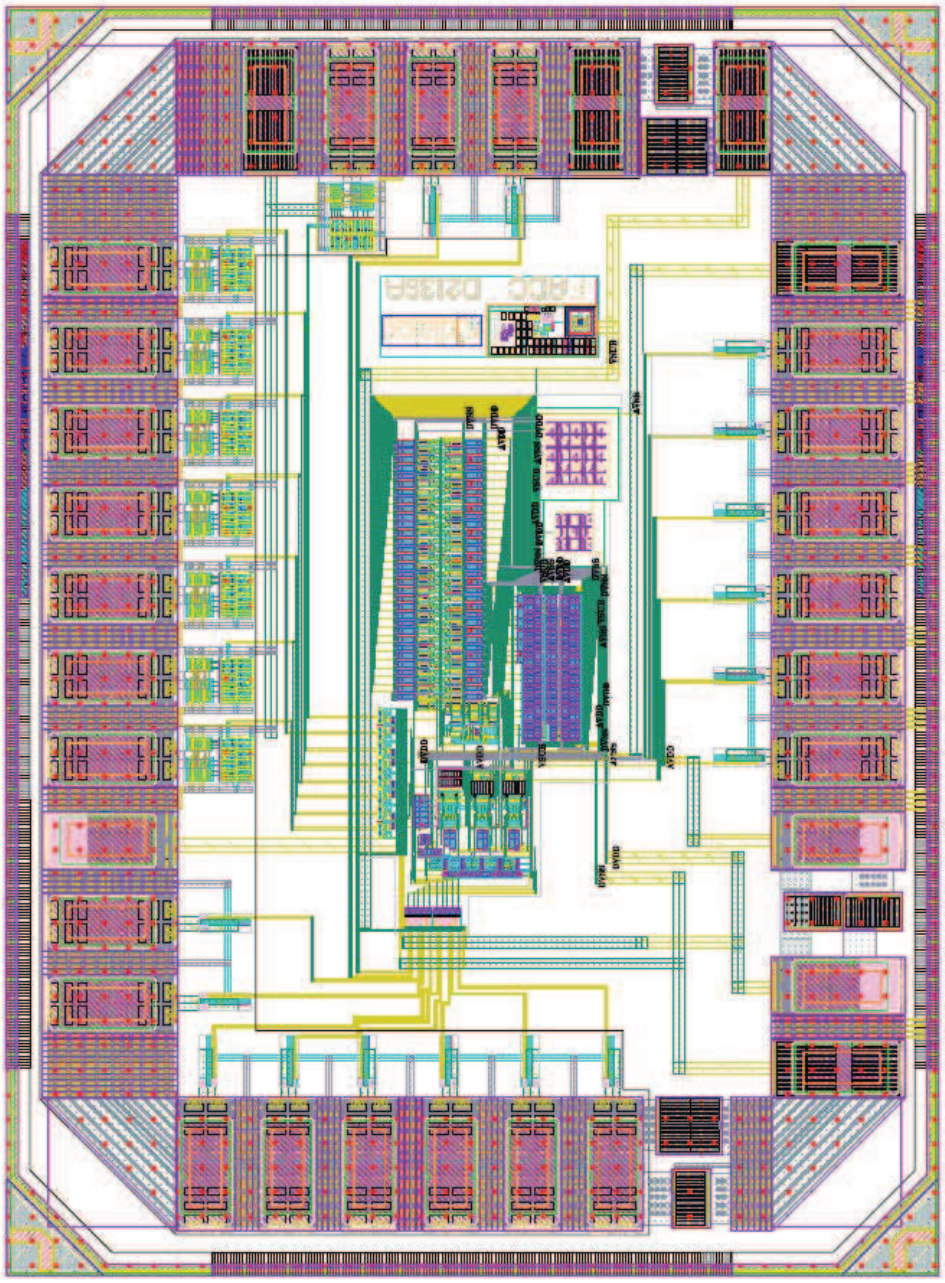

Figure 6.2: Top layout of the presented ADC

Table 6.1: List of pads

3.3V IO Supply Domain (IO)				
1.5V Analog Supply Domain (AS)				
1.5V Digital Supply Domaine (DS)				
Nr	PAD NAME	PAD TYPE	Domain	Description
1	DLY_SH	DIG_IN/STAT	IO	if 1 → shorter delay loop
2	CLK_IN	DIG_IN/DYN	IO	comp clock in (if CTRL_SW=1)
3	SYN_CLK	DIG_IN/DYN	IO	clock for sync of data out
4	SYN_MOD	DIG_IN/STAT	IO	if 1 → data out is sync to SYN_CLK
5	RES_IN	DIG_IN/STAT	IO	reset input for logic
6	CTRL_SW	DIG_IN/STAT	IO	if 1 → comp is clocked with CLK_IN
7	IDAC_OFF	DIG_IN/STAT	IO	test mode switch of the IDAC
8	DVSS	VSS 1.5 CORE	DS	digital ground
9	DVDD	VDD 1.5 CORE	DS	digital power supply 1.5V
10	AVDD	VDD 1.5 CORE	AS	analog power supply 1.5V
11	IB_ADC	ANALOG_IN	AS	current bias for IDAC
12	IB_CMP2	ANALOG_IN	AS	current bias for comp 2
13	IB_CMP1	ANALOG_IN	AS	current bias for comp 1
14	IB_CMP	ANALOG_IN	AS	current bias for main comp
15	VIN	ANALOG_IN	AS	input signal of fadc
16	CMPREF	ANALOG_IN	AS	ref voltage of comparator
17	AVSS	VSS 1.5 CORE	AS	analog ground
18	VSUB	SUB CORE	AS	substrate for analog and digital
19	IOVSUB	SUB IO	IO	IO substrate
20	DLY_MAN	DIG_IN/STAT	IO	if 1 → manual fast mode
21	CMPAUX_L	DIG_IN/STAT	IO	if 1 → aux comp low offset
22	CMP	DIG_OUT/DYN	IO	main comparator output
23	IOVSS	VSS 3.3 IO	IO	IO ground
24	CLK	DIG_IN/DYN	IO	clock for comparator
25	DOUT⟨0⟩	DIG_OUT/DYN	IO	digital output
26	DOUT⟨1⟩	DIG_OUT/DYN	IO	digital output
27	DOUT⟨2⟩	DIG_OUT/DYN	IO	digital output
28	DOUT⟨3⟩	DIG_OUT/DYN	IO	digital output
29	DOUT⟨4⟩	DIG_OUT/DYN	IO	digital output
30	DOUT⟨5⟩	DIG_OUT/DYN	IO	digital output
31	IOVDD	VDD 3.3 IO	IO	IO power supply 3.3V
32	DLY_FA	DIG_IN/STAT	IO	if 1 → fast mode (if DLY_MAN=1)

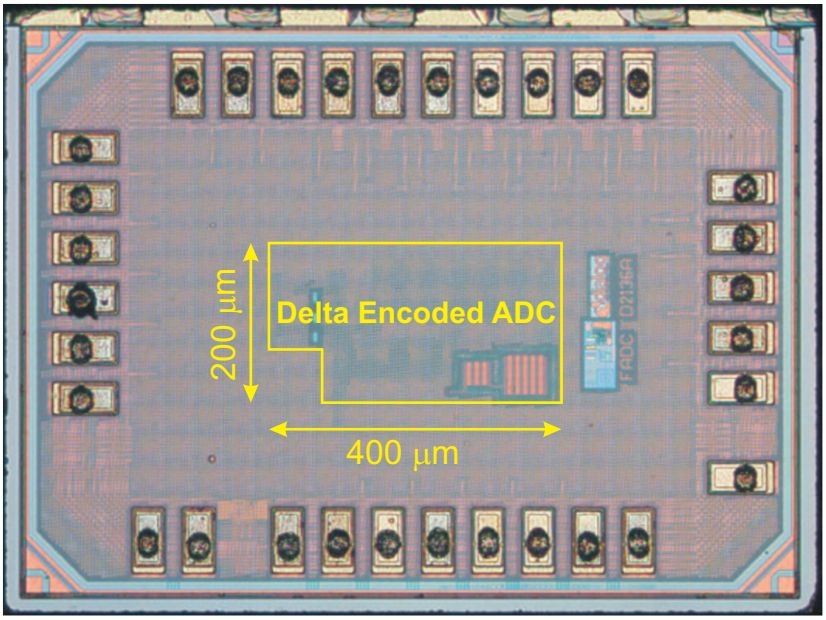

Figure 6.3: Microphoto of the proposed ADC

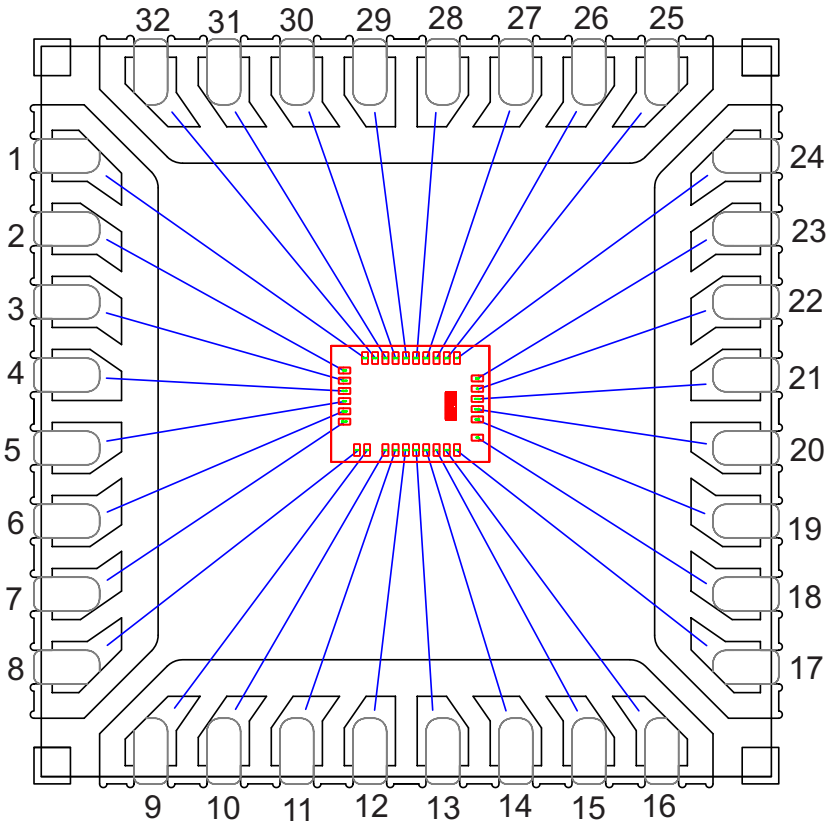

Figure 6.4: Packaging of the proposed ADC

6.2 Test setup

6.2.1 Self-clocked mode

The test setup in the self-clocked mode is shown in Fig. 6.5. The test equipments such as the clock generator and the power supply can produce much noise. So a low pass filter is integrated onto the test board, before the test signal is passed to the device under test (DUT). This reduces the noise level in the asynchronous as well as synchronous mode later.

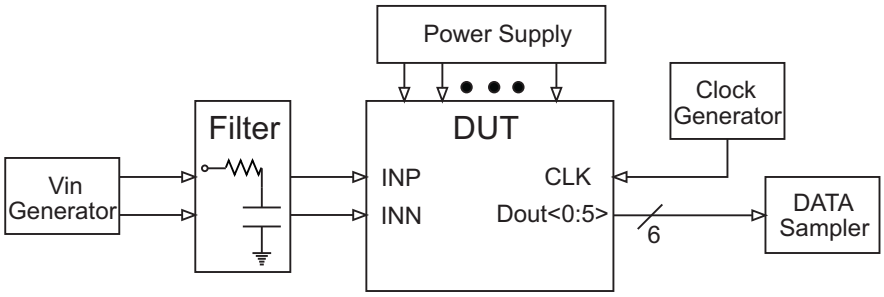

Figure 6.5: Test setup of ADC in self-clocked mode

The setup of the test chip and signal generators is listed in Table 6.2. In order to measure the ADC in the self-clocked mode, CTRL_SW is set to logic high. Each bias current is set to 2 μA and the reference voltage of the auxiliary comparator is set to 0.745 V. In addition, VIN is fed with a unit step signal of 85 mV. The power supplies of AVDD, DVDD and IOVDD are 1.4 V, 1.2 V and 2.5 V, respectively.

Table 6.2: Setup of DUT and signal generators

DUT/Signal Generator					
Pin	Value	Pin	Value	Pin	Value
CTRL_SW	1	CMPAUX_L	0	AVDD	1.4 V
SYN_MOD	0	IB_ADC	2 μA	DVDD	1.2 V
DLY_SSH	0	IB_CMP	2 μA	IOVDD	2.5 V
DLY_FA	0	IB_CMP1	2 μA	CMPREF	0.745 V
DLY_MAN	0	IB_CMP2	2 μA	VIN	85 mV

6.2.2 Dynamic measurement

The characteristics of static and dynamic linearity can only be verified and measured in synchronous mode. The basic setup for the measurement of the ADC is

Table 6.3: Test equipments

Vin Generator	Agilent 81150A Pulse function arbitrary waveform
Clock Generator	Agilent 81150A Pulse function arbitrary waveform
Power Supply	Keithley 2601 System source meter
DATA Sampler	LeCroy Waverunner 204 MXI Oscilloscope
Test System	ATX 7006, Applicos

presented in Fig. 6.6. In this measurement the ATX 7006 is used to provide the input signal, power supply and trigger for the ADC. At the same time the digital outputs of the ADC are sampled by the ATX 7006 to calculate the characteristics of its linearity, referred to the clock and input signals.

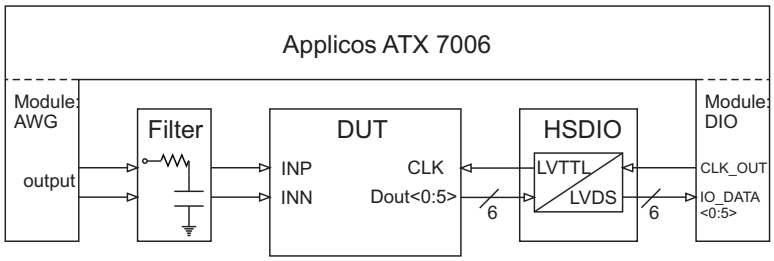

Figure 6.6: Test setup

In the synchronous mode the clock signal of the DUT is generated by the ATX 7006. After a certain timing delay, for example, 10 ns, the digital outputs of DUT are sampled and saved in ATX 7006. The high-speed, digital input-output adapter (HSDIO) is applied here for the transmission between digital outputs of the ADC and the ATX 7006. The digital output pads of this ADC have a driving capability of 10 pF. If the connection cable between the IO pins and ATX is too long, the large capacitance of the cable will defer the ADC characteristics. Therefore, HSDIO is used to enhance the driving capability.

6.3 Measurement result

6.3.1 Asynchronous characteristics

In contrast to a synchronous ADC, testing an asynchronous ADC with a sinusoidal input signal cannot demonstrate its characteristics. Especially the adaptive self-clocked frequency for tracking transient input signal cannot be shown. There-

fore, a unit step with 85 mV is applied to the ADC and the results are shown in Fig. 6.7.

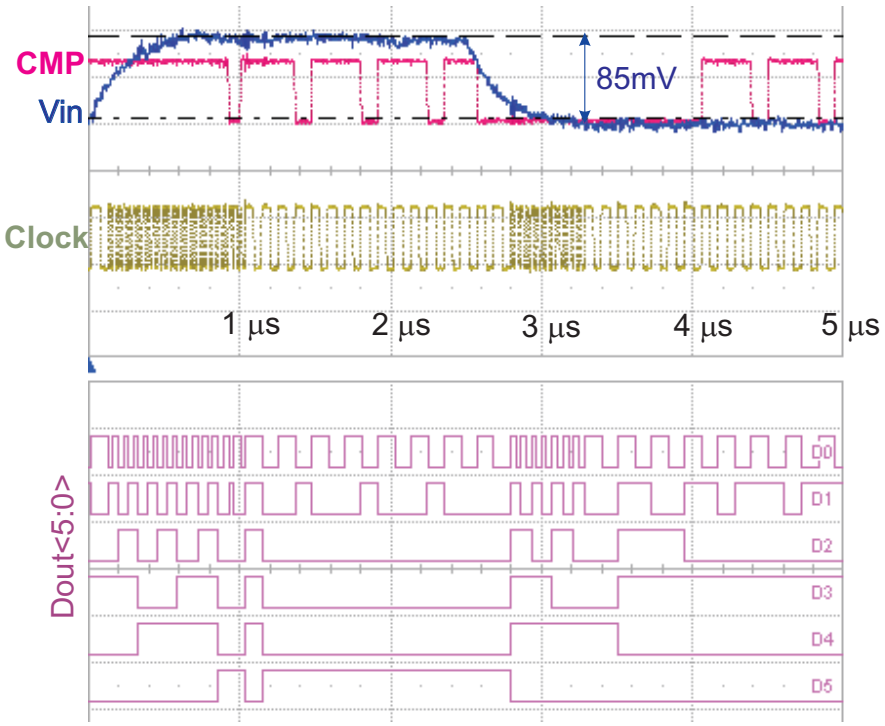

Figure 6.7: Self-adjustment of conversion rate

The diagram shows the main comparator output CMP, the input voltage step VIN, the input transient-dependent Clock, and the logic data out Dout$\langle 5:0 \rangle$. During the rising and falling slope of the input signal, the clock frequency, as well as the conversion rate, is increased automatically from 12.5 MHz to 50 MHz by the input transient detection. When the input signal is nearly stable, the clock frequency is decreased back down to 12.5 MHz.

6.3.2 Static linearity

The DC or static linearity of this ADC is measured in the synchronous mode. At a supply voltage of 1.4 V, a LSB voltage of 5 mV, and a unit current of 250 nA, the static characteristics of the ADC are demonstrated in Fig. 6.8 and Fig. 6.9.

The INL is less than a half LSB. This result confirms specifically that the statistical characteristics of the I-DAC indicated by the Eq. 5.5 match the requirements of the ADC. The real DNL should be larger than $+0.35/-0.32$ LSB

measured by the ATX 7006 from Applicos, where the noise is partially averaged by the measurement algorithm.

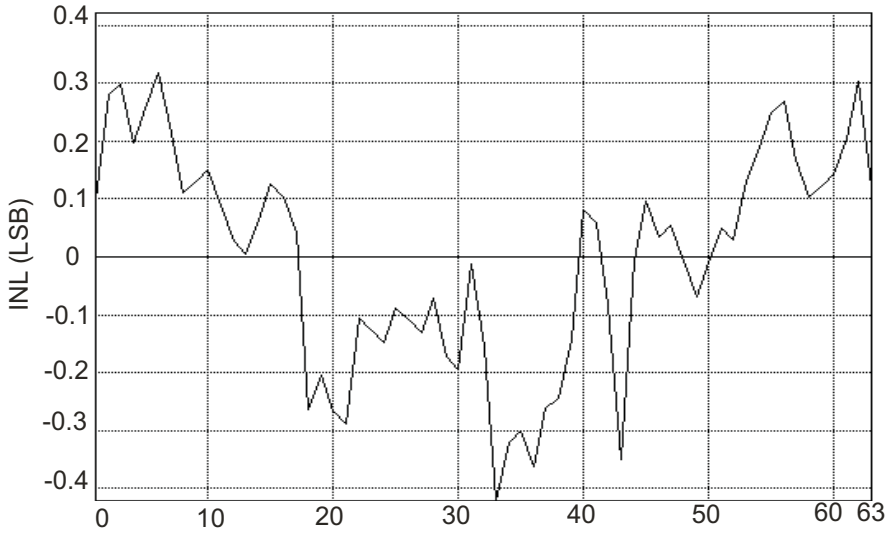

Figure 6.8: INL of the proposed ADC

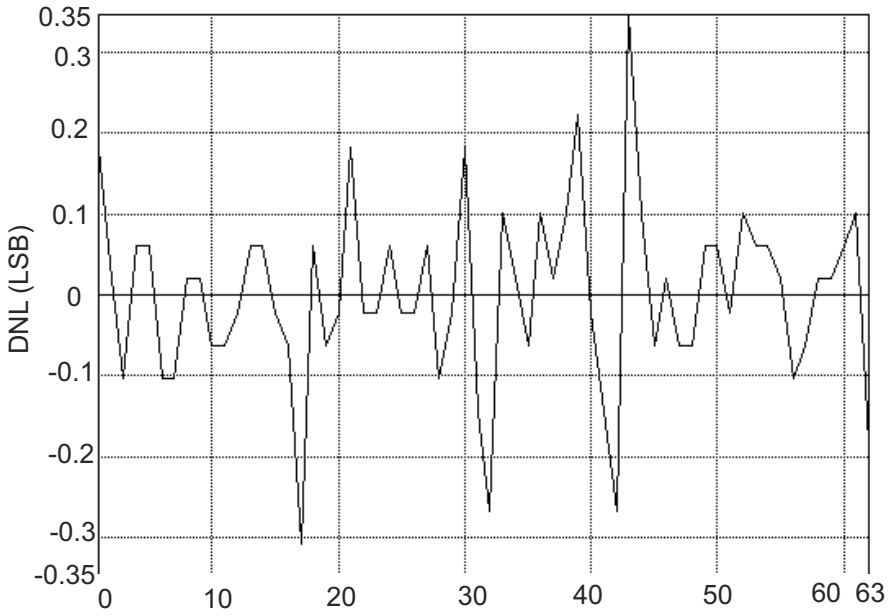

Figure 6.9: DNL of the proposed ADC

Moreover, the ATX provides also other approaches to verify the characteristics of static linearity. In Fig. 6.10 and Fig. 6.11 the characteristics of DC transfer demonstrate again that a monotone behavior of this ADC is achieved.

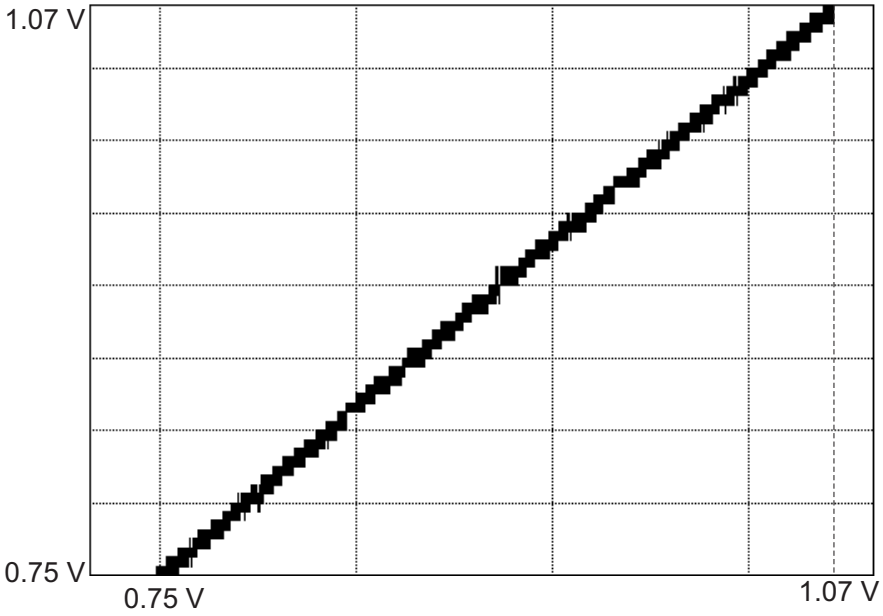

Figure 6.10: Ramp

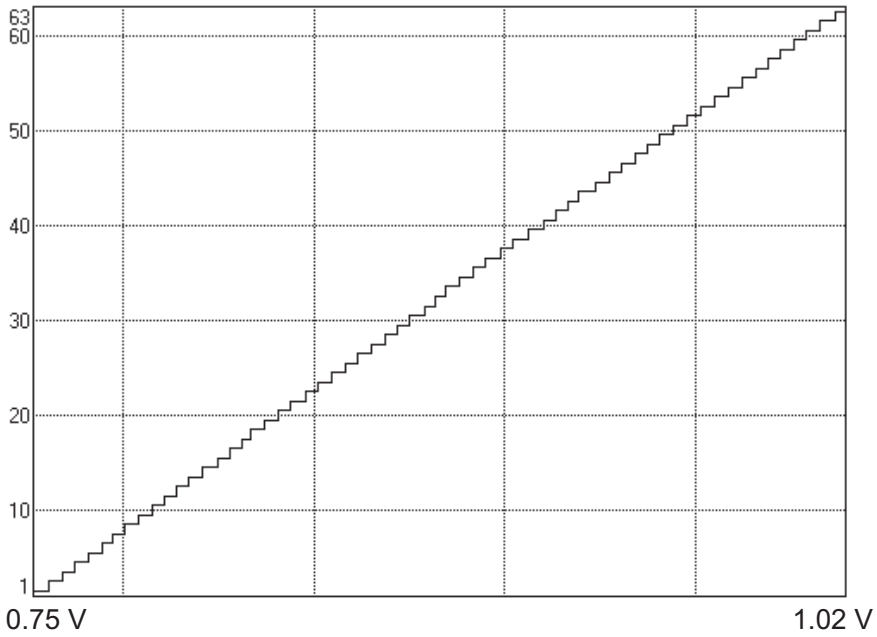

Figure 6.11: Transition point

6.3.3 Dynamic

A sinusoidal signal is applied to the ADC to evaluate the dynamic characteristics such as ENOB and SNR. Meanwhile, the internal clock as well as its digital outputs need to be triggered and sampled synchronously by the ATX 7006. The

ADC is clocked by the ATX 7006 at a frequency of 12.5 MHz − the nominal clock frequency. The input frequency is set to 62.5 kHz, which is defined by the maximum data slew rate of the ADC at the sampling frequency of 12.5 MHz. In this case, the consecutive tests are performed and the results are listed in Table 6.4.

Table 6.4: Dynamic characteristics of the ADC

	Value	Unit
Input Freq	62.5	kHz
THD	-48	dB
SFDR	49	dB
SNR	28.5	dB
ENOB	4.44	bits
Clk Freq	12.5	MHz

The dynamic performance of the ADC is characterized in Fig. 6.12, where a full swing sinusoid signal is applied to the input. The SFDR and SNDR are 49 dB and 28 dB, respectively. The ENOB is 4.4 bits, where the ideal ENOB that can be achieved is limited to 5 bits

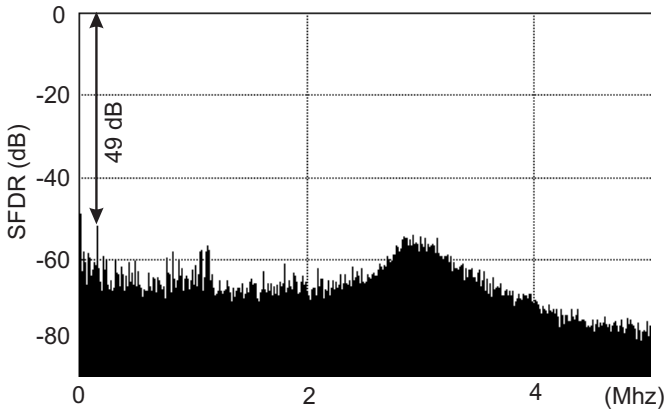

Figure 6.12: SFDR of the proposed ADC

6.4 Performance summary

Measurement results of this work along with the performance of similar ADCs using asynchronous processing or tracking techniques are summarized in Table 6.5.

It is determined that the clock density of 50 MS/s appearing in Fig. 6.7 is about 56%. So the average power dissipation in the time frame of Fig. 6.7 is 64 μW,

Table 6.5: Comparison of ADCs

	[40]	[47]	[65]	This work	
Process (nm)	130	180	65	130	
Supply (V)	1.2	0.7	1.2	1.4	
Resolution (bit)	6	8	6	6	
ENOB (bit)	5	6.9	5	4.4	
Sampling (MS/s)	300	0.05	500	12.5	50
Power (μW)	*105	25	*134	42	84
Area (mm^2)	0.06	0.96	0.056	0.08	
*Power consumption of single ADC is approximately estimated at 50 MS/s					

which is a reduction by 40% and 52%, compared to [40] and [65] respectively. The solution in [47] consumes comparable power (at a supply voltage of 0.7 V), but its sampling frequency is about a factor of 250 smaller than this work.

Chapter 7

Conclusion

7.1 Summary

A 6-bit delta-encoded Tracking ADC with transient-driven self-clocking is presented. The concept of the ADC is well suited for applications in digital controlled DC-DC converters, which require a short group delay and low power consumption.

A new design concept is proposed in this work, in which the ADC adapts its conversion rate to the requirements and characteristics of the DC-DC converters. Particularly, in steady-state of the DC-DC converter, when the output voltage of the DC-DC converters varies in a narrow band, the ADC is clocked at a slow sampling rate, resulting in lower power dissipation. Meanwhile, when a disturbance at the output of DC-DC converters occurs, this new ADC concept with cross-connected auxiliary comparators will automatically increase the data conversion rate, such that the ADC is able to respond to the signal variation synchronously and accurately.

A threshold window is applied for the detection of the tracking error, with the goal to decide whether the input signal variation is large or small. Two cross-connected auxiliary comparators with build-in offset voltage are implemented for that purpose. Depending on the requirements of applications, the offset voltage can be selected ranging from 10 mV to 30 mV. Furthermore, only one auxiliary comparator needs to be clocked with the main comparator, while the other auxiliary comparator is in the reset state, for additional reduction in power dissipation. The entire structure is easy to implement, since only one DAC feedback circuit is required. Compared to other topologies, e. g. using two capacitive DAC feedback circuits, this structure features a minimum chip area.

In addition, the small-signal modeling of the ADC is derived and calculated to guarantee the stability of the ADC feedback loop. The ADC is stable, when a following operation cycle is started by triggering the main comparator after settling of the DAC feedback loop in the current cycle. Otherwise the system cannot operate stable. However, the small-signal model does not feature large signal and dynamic characteristics. Therefore, the entire system is simulated by ScicosLab proving the dynamic behavior of the circuit. The simulation results of small-signal model, as well as in ScicosLab, confirm that the ADC is stable, reliable and feasible.

In terms of block level design the comparator is the key component, because the comparator determines the resolution of the ADC. In this work a new dynamic latched comparator is used, since it has a high power efficiency and low kickback noise characteristics. With the common mode input pair transistors the common mode kickback noise is significantly reduced below one third compared to a standard dynamic comparator. Additionally, differential kickback noise is reduced more than 50 % by using a new technique disconnecting the input stage from the latched output stage directly after triggering the latch. Kickback noise and thermal noise characteristics are analyzed by calculation and simulation. In this comparator the input-referred thermal noise is reduced to approximately one fourth compared to the standard dynamic latched comparator.

A transient noise simulation, which is particularly suitable for non-linear circuits, is used to explore the impact of thermal noise on the operation of the comparator. The noise model of the transistors of TSMC's 130 nm low power technology has been improved by sub circuits and additional noise sources. The noise model is adopted to the individual operating point and large signal operating switching point of the relevant transistors in the latched comparator and pre-amplifier stage. Using new noise models, the transient noise simulation reveal an input-referred effective thermal noise of only 3.6 mV. The accuracy is not impaired, because the LSB is specified with 5 mV. Based on new design features, the comparator achieves a minimum of kickback noise as well as thermal noise.

The entire system comprises other components like a voltage to current converter (VIC), a current steering DAC (I-DAC), a counter and other peripheral circuits for connection of the core circuit to the application. The I-DAC uses a unity architecture to achieve excellent DNL characteristics. However, it is still subject to INL limitations. The minimum dimensions of transistors are calculated, such

that an INL yield better than 99.7 % of the 6-bit DAC can be guaranteed. The matching characteristics are optimized by merging the unit cells of shift register with thermometer-coded I-DAC current source. The 64 unit cells are arranged symmetrically in a folded structure. The circuit is optimized for matching and low parasitic signal levels and reduced chip area. Monte-Carlo simulations of the I-DAC demonstrate standard deviations of 0.6 mV and the specifications of INL and DNL.

As proof of concept the 6-bit Tracking ADC is fabricated and measured, using integrated measurement equipment (ATX7006 from Applicos). At a sampling rate of 12.5 MHz and 50 MHz this ADC achieves a power consumption of 42 μW and 84 μW, respectively. The static characteristics, INL and DNL, are better than a half LSB. Application of a full scale sinusoidal input signal demonstrates a SFDR of 49 dB and a SNDR of 28 dB at 12.5 MHz sampling rate. The ENOB is 4.4 bits, whereas the theoretical ENOB of a 6-bit Tracking ADC is limited to 5 bits.

The objective of this work is to explore alternatives for the application of ADCs in the area of power management. In terms of digital-controlled DC-DC converters, high speed produces a high power consumption. In the world of synchronous circuits solutions are limited, even if many improvements have been achieved recently. But the essential issue, the direct dependence of power consumption and clock rate cannot be solved by synchronous data processing. This work demonstrates by measured data that the adaptive sampling rates can be used and a compromise between speed and power consumption can be achieved. As a result, the total average power consumption of the entire signal processing chain is considerably reduced.

7.2 Suggestion for future work

In an asynchronous system this ADC demonstrates the advantages that improve the issue of slope overload, from which the typical asynchronous ADCs [66] suffer. Meanwhile, the threshold window implemented in this work occupies less silicon area, achieving higher sampling rate but dissipating comparable power, when compared to [47].

To meet higher demands of other applications, one opportunity exists in exploring an adpative quantizer resolution. Also based on the slope of the input

transient, the quantizer resolution of the ADC could be automatically and nonlinearly adjusted, along with an adaptive sampling frequency. So that the issue of slope overload in the ADC can be further significantly improved.

A second option for optimizing this ADC performance is to combine both delay modes into one digital controlled delay line. The delay component in both delay modes in this ADC is implemented by the inverter. The two delay lines could be replaced by a delay line with adjustable and digitally controlled delay time. As the larger quantizer is selected in the ADC for the larger signal variation, a smaller delay time could be selected, resulting in a higher sampling frequency. Otherwise, at a low sampling frequency a smaller quantizer is adapted for slower signal variation. Therefore, the sampling rate of the ADC can nonlinearly vary in the defined frequency range. Meanwhile, by using this approach the ADC can provide more flexibility to meet the different demands in the applications.

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Declaration

I herewith declare that I have produced this thesis without the prohibited assistance of third parties and without making use of aids other than those specified; ideas and contribustions adopted directly or indirectly from other sources have been identified as such. This paper has not previously been presented in identical or similar form to any other German or foreign examination board.

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